



HAL
open science

Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies

M. Labrot, F. Cheynis, D. Barge, P. Maury, M. Juhel, S. Lagrasta, Pierre Müller

► **To cite this version:**

M. Labrot, F. Cheynis, D. Barge, P. Maury, M. Juhel, et al.. Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies. *Microelectronic Engineering*, 2017, 180, pp.56 - 64. 10.1016/j.mee.2017.04.009 . hal-01784096

HAL Id: hal-01784096

<https://amu.hal.science/hal-01784096>

Submitted on 3 May 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Accepted Manuscript

Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies

M. Labrot, F. Cheynis, D. Barge, P. Maury, M. Juhel, S. Lagrasta, P. Müller



PII: S0167-9317(17)30136-3
DOI: doi: [10.1016/j.mee.2017.04.009](https://doi.org/10.1016/j.mee.2017.04.009)
Reference: MEE 10514

To appear in: *Microelectronic Engineering*

Received date: 20 March 2017
Revised date: 6 April 2017
Accepted date: 11 April 2017

Please cite this article as: M. Labrot, F. Cheynis, D. Barge, P. Maury, M. Juhel, S. Lagrasta, P. Müller, Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies. The address for the corresponding author was captured as affiliation for all authors. Please check if appropriate. Mee(2017), doi: [10.1016/j.mee.2017.04.009](https://doi.org/10.1016/j.mee.2017.04.009)

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

M. Labrot^{a,b}, F.Cheyne^b, D.Barge^a, P.Maury^a, M.Juhel^a, S.Lagrasta^a, P.Müller^b

^aSTMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France.

^bAix Marseille Université, CNRS, CINaM UMR 7325, Case 913 campus de Luminy, 13288 Marseille cedex France.

Abstract

The Fully-Depleted Silicon-on-Insulator (FD-SOI) technology for advanced CMOS devices is based on SOI substrates formed by an ultra-thin Si or SiGe film on a thick insulator. A reduction of parasitic resistances of such CMOS components is obtained with the Raised Source and Drain (RSD) technology. In this work we show that modifying the SiconiTM plasma-based etching process widely used in microelectronic and/or combining it to wet-etching methods allows to improve the principal steps of fabrication of RSD FD-SOI CMOS devices.

More precisely, using sampling areas on 300 mm wafers that simulate the principal stages of FD-SOI building, (i) we show that a modified SiCoNi process may be used to increase the etching selectivity necessary to dissolve the oxide layer while maintaining a low-k spacer of high quality, (ii) we propose a combination of optimized SiCoNi-dry and wet etching that reduces the post-etching roughness and the contamination level of the channel surface before the subsequent epitaxy.

.....
Keywords: SiBCN, SiGe, SiCoNiTM Preclean, FD-SOI, Raised Source/Drain, WET clean

1. Introduction

The scaling of CMOS devices down to nanometric sizes has led to various integrations strategies to control short channel effects. Two distinct integrations are now clearly identified for technological nodes below 20 nm: FINFET integration [1, 2] and FD-SOI [3].

FDSOI integration requires the use of very thin channel materials, typically below 7 nm to obtain an accurate control of the channel [4, 5]. Such dimensions are inadequate for junction engineering in the source and drains, which thus needs to be raised by Epitaxy. This technique is commonly referred to as Raised Source Drain (RSD) in the literature [6].

Figure 1 schematizes the principal fabrication steps of RSD devices. The basic

brick for designing and building a FDSOI-based device consists in a SOI substrate formed by an ultra-thin Si or SiGe film, defining the device channel, on a thick insulator (BOX for buried oxide) bonded to a Si substrate. In the first steps of the process, the SOI substrate is topped by a 3D gate insulated from the channel by a High-K dielectric layer (HfO₂). The whole surface is covered with thin low-k dielectric layers (0p) of silicon nitride (typically Si₃N₄ or SiBCN). This step is followed by a photoresist coating which, after photolithography, exposes denuded zones for further etching of the low-k dielectric layers (step 2). The etching leaves resist residues that are removed by successive dry (plasma) and wet strips but leads to the formation of an oxide layer (step 3). The step 4 consists in removing the so-formed oxide layer (while avoiding any silicon nitride

consumption) followed by a surface cleaning. The last step (step 5) is the subsequent epitaxial growth of the SiGe:B raised source and drain.

Notice that conventional cleaning processes of SOI samples are usually based on high temperature treatments but such thermal treatments cannot be used for ultra-thin SOI films that, when heated, agglomerate in 3D islands [7, 8, 9, 10, 11, 12].

In Ref. [12] we proposed a new plasma-based cleaning methods (SiCoNi process) for SOI substrates that avoids any high temperature treatment. In this study, our goal is to go beyond this first approach and to integrate these etching and cleaning methods in the principal fabrication steps of SOI-based devices. From a methodological point of view, we focus in this study on the ultimate criterion to optimize the different technological steps involved in the RSD-epitaxy brick that consists in a careful comparison of the electrical performances of the devices fabricated with or without the optimized processes. Details regarding the targets for the different electrical performances and parameters can be found in Ref. [24]. In this paper, we will simply use, as an ultimate test, the increase of the number of active dies per cm² issued from the optimized process.

The paper, is divided in four parts: after a short presentation of the methodology, we describe the silicon nitride deposition (low-k dielectric layer), its etching properties and the queue time effect after etching (steps 1 and 2). In the third part we show how SiCoNi process may be modified to increase the SiO₂/silicon nitride etching selectivity (step 4). In the fourth part we show that a combination of wet and siconi-based methods enables to obtain a channel clean surface whose state (roughness, contamination, defectivity) enables a subsequent RSD epitaxy of good quality.

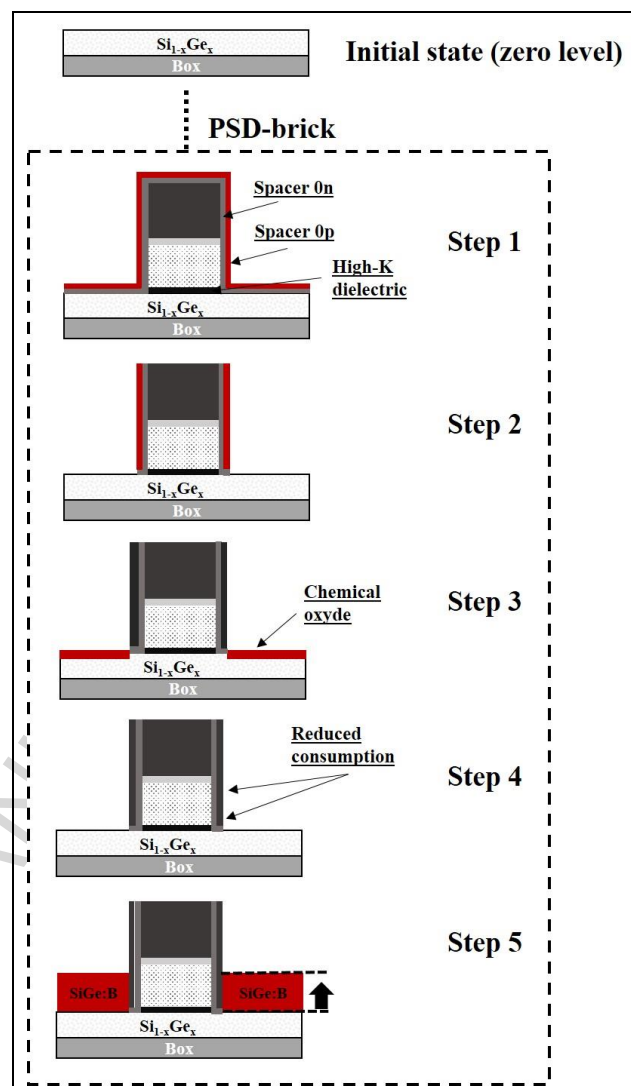


Figure 1: Initial state before gate fabrication and principal steps of fabrication of a FD-SOI based device from a basic gate-brick. Step 1/ Silicon nitride spacer coating, step 2/ Silicon nitride etching, step 3/ wet and dry strips with oxide formation, step 4/ surface cleaning (oxide removal without spacer consumption), step 5/ subsequent epitaxial growth of SiGe:B source and drain.

I/ Methodology:

I.1/ Simulation of the process

For the sake of simplicity we will not study real devices (characterized by complex 3D geometries) but will focus on planar surfaces that reproduce the successive technological processes including thin-film deposition, etch, clean... The so-studied samples (300 mm wafers) are described in Fig. 2. They simulate the initial SOI surface state (Fig. 2.2) exposing the channel surface,

the surface state after silicon nitride deposition (low-k dielectric layer deposition, Fig. 2.3), after the silicon nitride etching (Fig. 2.4), after the surface cleaning including the formation and the removal of a wet oxide layer (Fig. 2.5) and after the subsequent epitaxy of $\text{Si}_{1-x}\text{Ge}_x\text{:B}$ epitaxy defining the RSD layer.

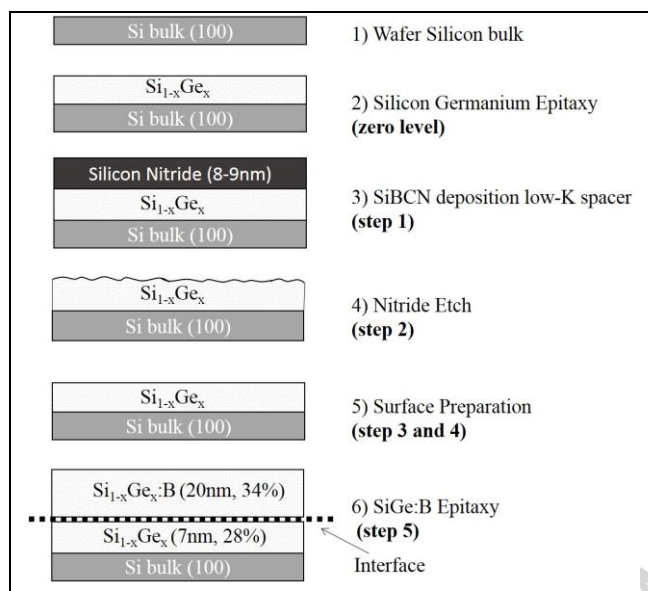


Figure 2: Description of different SiGe samples (300 mm SOI wafer) under study: 1) initial silicon bulk used as a reference material, 2) SiGe layer grown by epitaxy (channel layer), 3) nitride silicon deposition (low-k dielectric layer), 4) silicon nitride etching, 5) surfaces cleaned by various processes, 6) SiGe:B layer grown by epitaxy (Raised-Source-Drain epitaxy). The steps in bracket correspond to figure 1.

I.2/ Methods:

We will use various dry and wet cleaning processes reported in table 1 and detailed in appendix A: 1: HF-rinse-and dry (called ‘HF last’), 2: SiCoNi Preclean, 3: HF-RCA, 4: HF-last + SiCoNi , 5: HF-RCA+ SiCoNi .

Process	Description	Passivation	Chemical Oxide
1	HF last	-H	No
2	SiCoNi Preclean (NH_4F)	-H	No
3	HF-RCA	-OH	Yes
4	HF-last + SiCoNi	-H	No
5	HF-RCA + SiCoNi	-H	No

Table 1: Description of the different processes used in this work to prepare the surface in step 5 in Fig.2.

The cleaned and uncleaned surfaces are characterized by measuring their roughness, defectivity and chemical composition by using classical tools described in table 2. (for more details the reader is referred to [12]).

Acronym	Name	Measured parameter
AFM	Atomic Force Microscopy	Root mean square roughness
SE	Spectroscopic Ellipsometry	Effective index
XPS	X-ray photoelectron spectroscopy	Chemical analysis
SIMS	Secondary Ion Mass Spectrometry	Chemical analysis
SEM	Scanning Electron Microscopy	Local morphology (defects)
SIR	Spectroscopic Infra-Red Reflectometry	Particle contamination

Table 2: Methods of analysis used in this work.

II/ Optimization of step 2: silicon nitride deposition and etching

II.1/ Silicon nitride choice

For CMOS technologies, oxide or nitride dielectrics are used to encapsulate and isolate the gate laterally (Fig. 1 step 1, see appendix B for details regarding the dielectric layer deposition). These dielectric layer also has a spacer function to precisely localize dopant implantations and subsequent RSD epitaxial growth close to the gate. Since these doped regions must be very close to the channel, the spacer has to be as thin as possible. The lower limit of the thickness can be reduced by using low permittivity material. Other criteria have to be taken into consideration to choose the dielectric material. It should resist to HF etching and should not oxidize. Si_3N_4 silicon nitride is standardly used in CMOS technology as a low-k dielectectric. However, boron decreases the silicon nitride permittivity and carbon increases its resistance to HF etching [13]. Consequently SiBCN coating has been considered in the present work as it decreases the effective capacitance of the spacer (permittivity of 5.2 instead of 7.5 for Si_3N_4) and improves by 10% the performance and speed of the final transistor compared to standard nitride spacer [14].

II.2/ Silicon nitride characterization after deposit

Figure 3 shows AFM images and RMS measurements of surfaces after nitride deposition. The measured roughness is smaller for Si_3N_4 than for SiBCN by almost a factor 2. Such a difference is essentially due to the grain size. Indeed despite a polycrystalline configuration for both materials, SiBCN forms larger grains than Si_3N_4 (see AFM pictures) [13, 14].

The surface defectivity measured by SIR is greater for SiBCN than for Si_3N_4 (~30 defects per wafer). Despite its greater defectivity, SiBCN material shows better performance (permittivity and etching selectivity - see section III). As a result, we will use SiBCN as a dielectric spacer in the following.

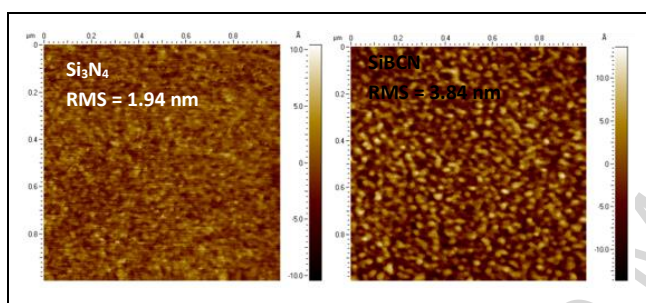


Figure 3: $1\ \mu\text{m} \times 1\ \mu\text{m}$ atomic force microscopy images associated with different types of silicon nitride surface.

II.3/ Silicon nitride etching and queue time impact

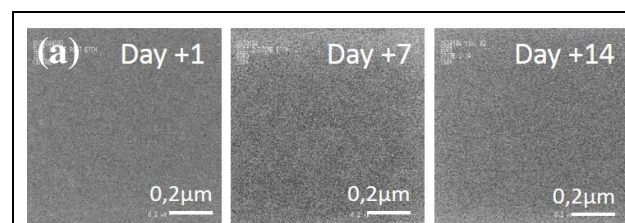
In CMOS technology, the removal of the silicon nitride film (step 2) is a critical step as it represents a possible source of device damages. Indeed a possible over-etch of the nitride may result in damages of a thin oxide and the underlying silicon substrate [15]. For this purpose, in industrial conditions, the etching is generally realized in two stages: a quick etching stage followed by a slow selective etching stage. This procedure avoids corner effects at the vertical-spacer/channel junction and thus helps to obtain a vertical spacer with a constant thickness. In the case under study (simulation process) we only use the quick etching stage. The silicon nitride etching (Fig. 1 step 2) consists in dry/etch based on N_2/O_2 plasma.

For practical reasons, there is always a queue time between the etching (step 2) and the

surface preparation before the RSD deposition (Fig. 1 step 5). During this queue time the surface may degrade by surface contamination and/or oxidation. This queue-time cannot be reduced to zero. We thus study the influence of the queue time on the surface defects (Fig.4) and on the surface roughness (Fig. 5). As shown in Fig 4, the etching may leave polymers defects (typically CF_xH , CF_xN , CF_xO) and resin residues (CH-CH) on the surface. Due to their high volatility these residues may partially disappear during the queue time. It is for instance the case for fluoride components which reduce by a factor 2 for queue times of 14 days (see table 3). However, at smaller scale, polymers tracks remain, so the surface has to be cleaned by wet and dry strips [16].

In Figure 5 we report the RMS height variation measured just after the silicon nitride etching when the wet/dry strips have been carried out right after the nitride etch or after a queue-time. As evidenced in Fig 5, (i) the RMS post etching are similar for SiGe and silicon channels ($\text{RMS} = 0.15 \pm 0.01\ \text{nm}$), (ii) the roughening induced by the cleaning (dry + wet) does not change for SiGe but roughly increases by a factor 3 for silicon (the SiCoNi plasma is known to degrade more silicon than germanium surface [15]), (iii) the queue-time affects more the SiGe surface than the already degraded Si surface.

The main contaminants (F, O and C) detected by XPS are reported in Table 3. Contrary to fluorine which desorbs during the queue-times, carbon and oxygen contaminations slightly increase with time.



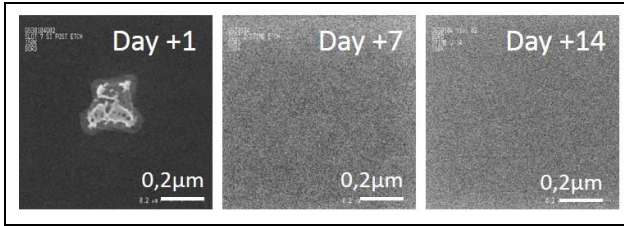


Figure 4: Top view SEM images after post nitride etching of surface evolution for different day (queue-times impact) (a) on SiGe epitaxy, (b) on Si (100). In this last case (b) a polymer residue observed just after etching spontaneously desorbs during queue-times and thus disappears on the SEM images.

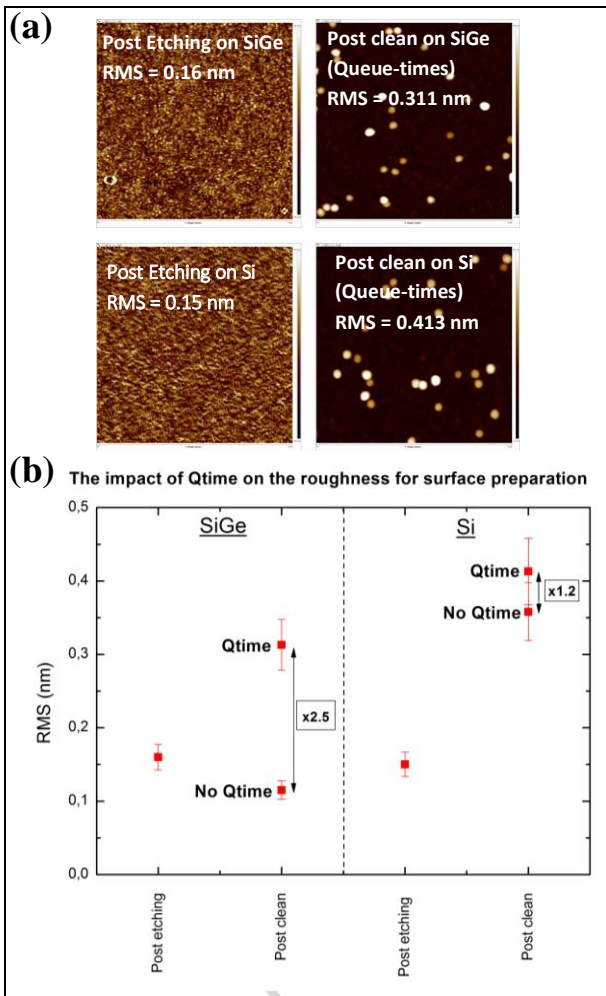


Figure 5: (a) $1 \mu\text{m} \times 1 \mu\text{m}$ atomic force microscopy images associated with post nitride etching on Si(0 0 1) and SiGe epitaxy. (b) RMS value on different Si/Oxide and SiGe/oxide interfaces for different treatments (Post Etching, Post clean with queue-times (day +14) and no queue-time).

Surface	Process	Contaminations
Si	Post etching	C (5%), O (18%), F (20%)
	Day +7	C (6%), O (20%), F (11%)
	Day +14	C (8%), O (22%), F (10%)
	Post wet	C (1%), O (22%), F (4%)
Si	<u>Reference (post wet)</u>	<u>F(<1%), O and C (detection limit)</u>

SiGe	Post etching	C (4%), O (17%), F (18%)
	Day +7	C (5%), O (18%), F (9%)
	Day +14	C (6%), O (18%), F (8%)
	Post wet	C (<1%), O (18%), F (2%)
SiGe	<u>Reference (post wet)</u>	<u>F(<1%), O and C (detection limit)</u>

Table 3: Synthesis of chemical contaminations of the Si and SiGe surface for different queue-times. The results is compared for reference with no queue-times.

Finally, notice that, the surface contamination has a huge effect on the subsequent epitaxy. For instance we report in Fig. 7 SEM images obtained after subsequent epitaxy of SiGe:B on these contaminated surfaces. Since the epitaxy enlarges the surface defects [12] the queue time drastically decreases the quality of the epitaxial layer. Such large defects correspond to bright spots in post-clean AFM images in Fig.5.

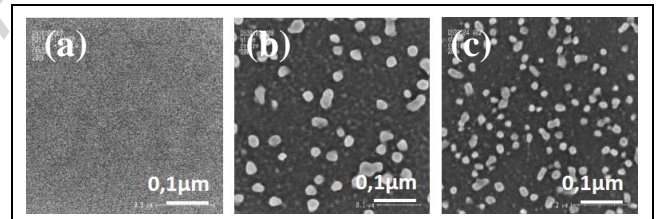


Figure 6: Top view SEM images after SiGe:B epitaxy. (a) Raised source and drain reference epitaxy (SiGe:B) with no queue-time, (b) Epitaxy (SiGe:B) raised source and drain on Si with queue-times (Day +14), (c) Epitaxy (SiGe:B) raised source and drain on SiGe with queue-times (Day +14).

III/ Optimization of step 4: SiO₂/silicon nitride etching selectivity

As shown in Fig 1, step 4 consists in etching the SiO₂ film with a minimum consumption of the silicon nitride (Si₃N₄ or SiBCN) that forms the vertical/lateral spacer. Since Siconi technology is already used in industrial conditions, we propose to optimize the Siconi process to increase the etching rate ratio (SiO₂ over silicon nitride).

For this purpose the experimental parameters of the SiCoNi process have been varied around

their standard-recommended values according to a well-known design of experiments (DOE, see appendix C for details) [17]. The etching ratios, obtained with each process, have been evaluated from thickness change measurements by spectroscopic ellipsometry. The etching rates are reported in Table 4 for different set of experimental parameters (Si_3N_4), by varying the NF_3/NH_3 flux ratio, the etching temperature and the heating time to remove the $(\text{NH}_4)_2\text{SiF}_6$ salt formed during the SiCoNi process [12]. For comparison usual standards SiCoNi conditions for Si_3N_4 and SiBCN correspond to the last two processes in table 4.

Process	NF_3/NH_3 ratio (scm)	Etch Temp. (°C)	Heating Time (s)	Selectivity
1	~1:10	35	120	8.5
2	~1:8	35	60	9.8
3	~1:35	35	60	6.8
4	~1:12	35	120	9.3
5	~1:15	32,5	90	9.3
6	~1:15	32,5	90	9.6
7	~1:15	32,5	90	9.5
8	~1:10	30	60	8.7
9	~1:8	30	120	12.5
10	~1:35	30	120	8.8
11	~1:12	30	60	12.1
$\text{SiO}_2/\text{Si}_3\text{N}_4$	Standard conditions			5.0
$\text{SiO}_2/\text{SiBCN}$	Standard conditions			9.5

Table 4: Description of the various SiCoNi processes checked in this study with the used parameters. The last column shows the selectivity obtained for each process.

The results show that the selectivity decreases with a reduction of the NF_3 gas flow with respect to the NH_3 (compare for instance processes 2 and 3 or 9 and 10). The selectivity rate increases with the temperature. The heating time does not have any impact on the selectivity, but a minimum time must be kept for salt desorption. The results, synthesized in Fig. 7, unambiguously show that the best selectivity is achieved for process 9 of Table 4, i.e. with low temperature and high gas flow. Moreover for a given process (reference process) a better selectivity is achieved with SiBCN than with Si_3N_4 .

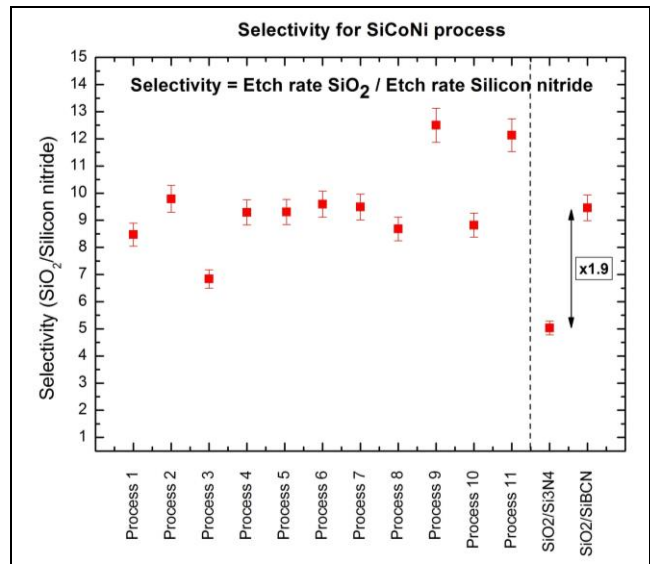


Figure 7: Study of selectivity ($\text{SiO}_2/\text{Silicon nitride}$) for different process SiCoNi. In the right part we compare the selectivity for SiBCN and Si_3N_4 materials (error bars correspond to statistic errors).

Beyond the etching selectivity, the different processes, described in Table 4, lead to different surface states that have been characterized by SIR and are described in Table 5. We artificially divide the defects in two populations: "Small defects" ($40 \text{ nm} < x \leq 150 \text{ nm}$) and "large defects" ($150 \text{ nm} < x \leq 1 \mu\text{m}$). The number of defects increases for lower temperatures and higher NF_3/NH_3 flow ratio but still remains fully compatible with device working conditions for all reported samples.

Process	$T_{\text{etch}}=35^\circ\text{C}$		$T_{\text{etch}}=32,5^\circ\text{C}$		$T_{\text{etch}}=30^\circ\text{C}$	
	small defect	big defect	small defect	big defect	small defect	big defect
1, 5, 8	11	2	13	4	24	3
2, 6, 9	12	4	8	1	8	1
3, 7, 10	5	3	5	1	25	27
4, 11	7	2			15	3

Table 5: Total number of defects on a 300 mm wafer measured for various processes.

IV/ Optimization of step 5: combination of wet and dry cleanings to improve the channel surface quality

Throughout the successive technological steps, the devices to-be are

regularly cleaned. It is especially the case of the channel surface on which any defect may be detrimental for subsequent source and drain epitaxy. Based on our previous work [12] on the optimization of the surface cleaning of a SOI wafer (zero level in Fig 1) we compare the states (roughness, contamination, defectivity) of the channel surface that result from various combinations of wet and SiCoNi-based dry cleanings.

All the experimental results are compared to a reference process that corresponds to a surface simply exposed to HF-RCA + SiCoNi treatment (best cleaning treatment for the initial stage depicted in Fig. 2 [12]).

IV.1/ Comparison of surface defectivity before and after cleaning

Figure 8 shows the total number of defects (measured by SIR) after nitride deposition, after nitride etching and after different cleaning processes. After silicon nitride deposition and etching, the number of defects remains low for both Si and SiGe surfaces. For most of the tested clean combinations, the surface defectivity remains comparable with the reference process. Only the single SiCoNi clean produces a significant larger number of defects. However when combined with the HF-last process (HF-last+SiCoNi), the resulting surface exhibits a number of defects per wafer lowered by a factor 2 with respect to the reference process (HF RCA+SiCoNi).

The benefit of SiCoNi is thus clearly evidenced: without SiCoNi cleaning the defectivity is above $4 \text{ defects.cm}^{-2}$ and with the SiCoNi process, this number is reduced to less than $0.1 \text{ defect.cm}^{-2}$.

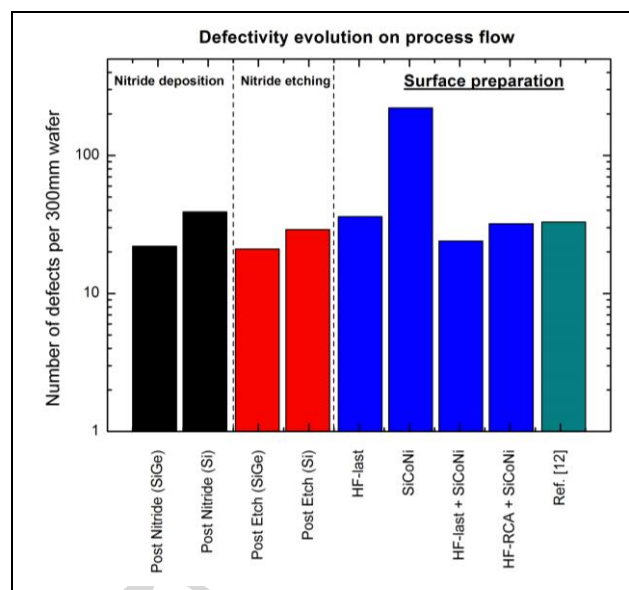


Figure 8: Total number of defects on a 300 mm wafer measured in different conditions that means after nitride deposition (step 1) (black), after nitride etching (step2) (red), and after surface cleaning (step 4) by wet cleans, plasma cleans and combination of both for SiGe.

IV.2/ Surface contamination induced by the cleaning processes

A quantitative analysis of the surface residual contamination due to cleaning processes is not easy to perform since in our experimental conditions we transfer the sample from the cleaning chamber to another chamber equipped with analytical tools. This transfer may contribute to surface contamination. The surface contamination has thus been analyzed by SIMS on capped films that means after subsequent epitaxy of a protective layer (SiGeB in our case).

The SIMS concentration profiles $I(z)$, where z is the analysis depth normalized to the thickness of the SiGe:B epitaxial deposit, obtained after the different cleaning processes are reported in Fig 9. The surface of the epitaxially grown film corresponds to $z=0$ while the location of the initial cleaned surface (before being further embedded by protective epitaxy) corresponds now to the interface located at $z=1$. For the sake of clarity, the SIMS profiles corresponding to different cleaning processes have been vertically shifted.

According to the cleaning process various residual contaminants have been detected. They are reported in Table 6 and

essentially correspond to C, O, Cl and F. We can see that most of the cleaning methods, excepted the HF-RCA+SiCoNi and HF-last process, lead to a surface contamination greater than the one measured on the reference sample cleaned by HF-RCA+SiCoNi [12].

Notice that the F contamination, and the residual associated roughness, may be reduced by a decrease of the queue time between the formation of the $(\text{NH}_4)_2\text{SiF}_6$ salt and its desorption during the SiCoNi process (see ref [12]).

Process	Contaminations (at/cm^2) (SIMS)			
	Carbon	Oxygen	Fluor	Chlorine
HF-last	No	Detection limits	No	No
SiCoNi	$1.0 \cdot 10^{11}$	No	$3.0 \cdot 10^{12}$	$3.5 \cdot 10^{12}$
HF-last + SiCoNi	$2.9 \cdot 10^{12}$	No	$5.1 \cdot 10^{11}$	$1.5 \cdot 10^{12}$
HF-RCA + SiCoNi	$3.7 \cdot 10^{10}$	No	No	$1.0 \cdot 10^{10}$
HF-RCA + SiCoNi [12]	No	No	No	$2.0 \cdot 10^9$

Table 6: Chemical contaminations of the SiGe/SiGe:B interface for different surface preparations as determined by SIMS.

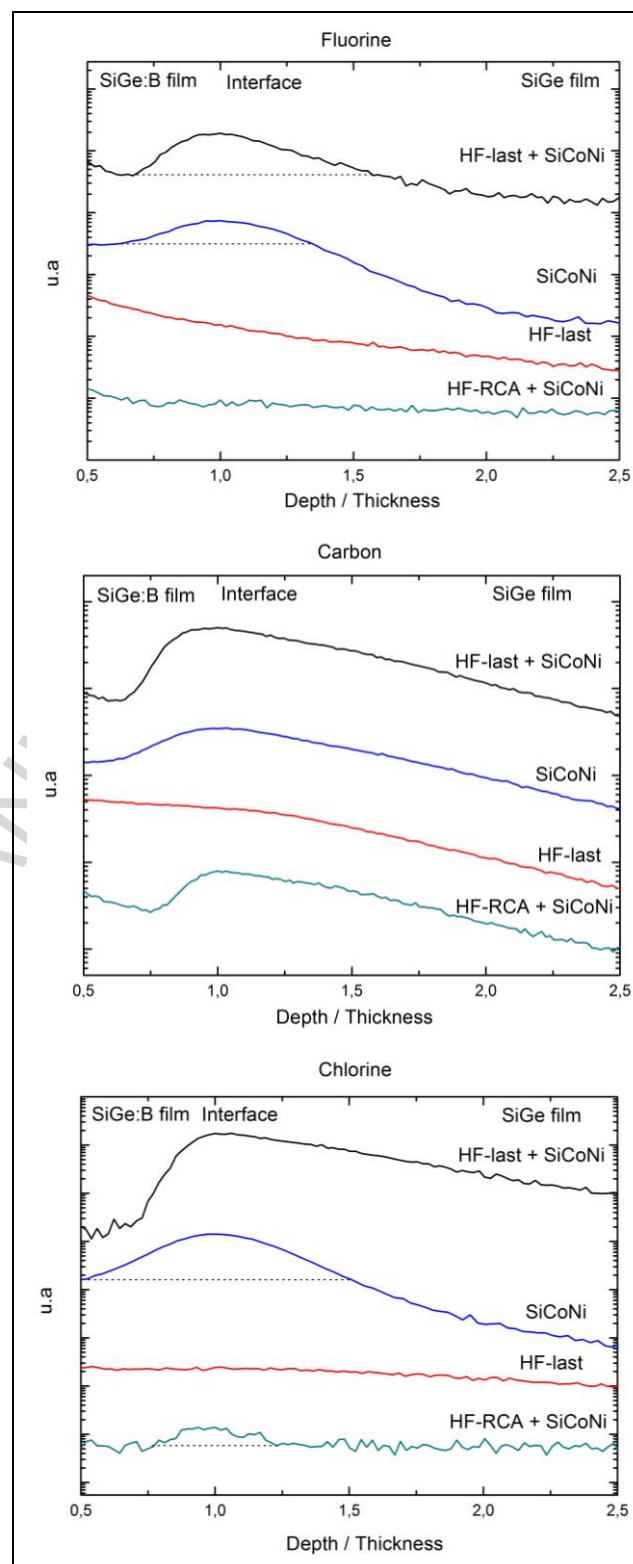
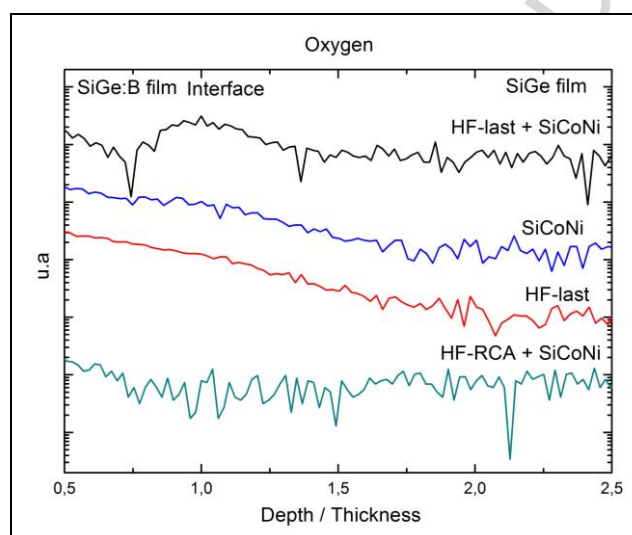


Figure 9: SIMS depth profiles of the F, C, Cl and O atoms in SiGe/SiGe:B interface.

IV.3/ Synthesis

Table 7 synthesizes the main results. In terms of defectivity, contamination at the SiGe/SiGe:B interface (channel/RSD interface)

and morphology, the best surface state is reached with HF RCA + SiCoNi.

Even if the SIMS profiles are slightly wider in this study than those reported in [12], the final surface state is comparable to the one obtained by the standard low temperature treatment used for SiGe in its bulk configuration [12].

Process	Defectivity	Contamination	Morphology
HF-last	☺	☺	☺
SiCoNi Preclean	☺	☺	☺
HF-last + SiCoNi	☺	☺	☺
HF-RCA + SiCoNi	☺	☺	☺

Table 7: Synthesis of experimental results for different surface preparations of SiGe surface.

VII/ Improvement of electrical devices

Electrical performances have been measured on an ensemble of MOSFET transistors. More precisely characteristics in current and tension, leakage currents, carrier mobility, access resistance and capacity values have been measured. They are reported in Ref. [24]. The characteristics of the optimized devices all belong to the targeted values which have been standardly defined as a prerequisite for being used in electronic industry (ITRS roadmap). The ultimate test is the number of active dies per wafer, that means the number of dies that perfectly fit the functioning zone. This analysis show a huge enhancement of this percentage since the number of electrical active devices increases from 40 % to 90 %.

VIII/ Conclusion

Studying planar surfaces that simulate the principal steps of fabrication of FD-SOI based devices, we have been able to optimize the conditions to epitaxially grow Raised Source and Drain. More precisely we show that:

(1) The best silicide to be used is SiBCN.

(2) The SiCoNi process may be adapted to control the SiO₂/Silicon nitride etching selectivity.

(3) The queue time between nitride etching and surface cleaning has to be reduced to avoid surface contamination,

(4) The best surface preparation for raised source and drain integration in FD-SOI devices is the HF-RCA + SiCoNi (process 9 in table 3). Such a low thermal budget process corresponds to an optimized version of the method proposed in Ref. [12] and avoids any dewetting of the channel in the experimental conditions used.

(5) Analysis of electrical devices show that all these improvements lead to a doubling of the percentage of electrical active dies per wafer.

The so proposed recipes developed for blanket wafers may be easily transferred to real patterned substrate to reach high quality CMOS devices as shown in Fig. 10.

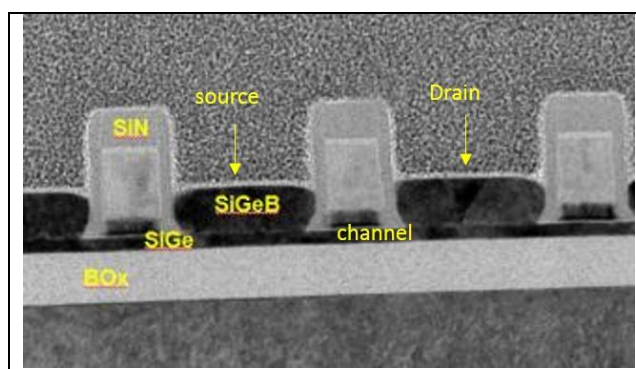


Figure 10 – CMOS FD-SOI devices obtained from the optimized processes described in this paper.

Acknowledgements

This work was supported by ANRT N°1030/2013.

References

- [1] J.L. Autran, D. Munteanu, *Revue de l'Electricité et de l'Electronique*, (2003), no. 8, p. 21-31.
- [2] J.L. Autran, D. Munteanu, *Revue de l'Electricité et de l'Electronique*, (2007), no. 4, p. 25-37.
- [3] N. Loubet, T. Adam, M. Raymond, Q. Liu, K. Cheng, R. Sreenivasan, A. Reznicek, P. Khare, W. Kleemeier, V. Paruchuri, B. Doris, and R. Sampson. *Thin Solid Films* 520 (2012) P3149-P3159.
- [4] Violette, K. E., C. P. Chao, R. Wise and S. Unnikrishnan, *Journal of the Electrochemical Society*, 146 (5), (1999) p. 1895.
- [5] T. Uchino, T. Shiba, K. Ohnishi, A. Myauchi, M. Nakata, Y. Inoue, and T. Suzuki, 1997 IEDM Technical Digest, (1997) p. 479.
- [6] J.M Hartmann, V. Benevent, A. Andre, C. Sirisopanaporn, M. Veillerot, M. P. Samson, S. Barraud, Z. Essa, and B. Sermage. *ECS Journal of Solid State Science and Technology*, 3 (11) (2014) P382-P390.
- [7] F. Cheynis, F. Leroy, P. Müller, C. R. *Physique* 7 (2013) p. 578.
- [8] E. Jiran, C. Thompson, *J. Electr. Mater.* 19 (1990) p. 1153.
- [9] D. Danielson, D. Sparacin, J. Michel, L. Kimerling, *J. Appl. Phys.* 100 (2006) 083507.
- [10] F. Cheynis, E. Bussmann, F. Leroy, T. Passanante, P. Müller, *Phys. Rev. B* 84 (2011) 245439.
- [11] F. Leroy, F. Cheynis, T. Passanante, P. Müller, *Phys. Rev. B* 88 (2013) 035306.
- [12] M. Labrot, F. Cheynis, D. Barge, P. Müller, M. Juhel, *Applied Surface Science* 371, (2016) P436–446.
- [13] O. Weber, E. Josse, F. Andrieu, A. Cros, E. Richard, P. Perreau, E. Baylac, N. Degors, C. Gallon, E. Perrin, S. Chhun, E. Petitprez, S. Delmedico, J. Simon, G. Druais, S. Lasserre, J. Mazurier, N. Guillot, E. Bernard, R. Bianchini, L. Parmigiani, X. Gerard, C. Pribat, O. Gourhant, F. Abbate, C. Gaumer, V. Beugin, P. Gouraud, P. Maury, S. Lagrasta, D. Barge, N. Loubet, R. Beneyton, D. Benoit, S. Zoll, J. D. Chapon, L. Babaud, M. Bidaud, M. Gregoire, C. Monget, B. Le-Gratiet, P. Brun, M. Mellier, A. Pofelski, L. R. Clement, R. Bingert, S. Puget, J. F. Kruck, D. Hoguet, P. Scheer, T. Poiroux, J. P. Manceau, M. Rafik, D. Rideau, M. A. Jaud, J. Lacord, F. Monsieur, L. Grenouillet, M. Vinet, Q. Liu, B. Doris, M. Celik, S. P. Fetterolf, O. Faynot, M. Haond, *VLSI* (2014) 14582357.
- [14] E. Josse, J. Mazurier, N. Degors, S. Chhun, P. Maury, S. Lagrasta, D. Barge, J. P. Manceau, M. Haond, *VLSI* (2015) 15412567.
- [15] Kazuo Nojiri, *Dry Etching Technology for Semiconductors*, Springer (2014).
- [16] C. Gabriel, M. Weling, *The Electrochemical Society* (1993), p235-242.
- [17] Friedrich Pukelsheim, *Optimal Design of experiments*, SIAM (editor), (2006).
- [18] H Yang, X Lu, CT Kao, M Chang – US Patent 7,780,793 (2010).
- [19] R Arghavani, CT Kao, X Lu - US Patent 7,955,510 (2011).

[20] E.I. Mel'nichenko, G. F. Krysenko, D. G. Epov; Russian journal of inorganic chemistry, vol. 50, no2, (2005) pp. 153-157.

[21] E.I. Mel'nichenko, G. F. Krysenko, D. G. Epov, and E.Yu. Marusova. Russian journal of inorganic chemistry 2004, vol. 49, no12, pp. 1803-1806.

[22] A. Fukazawa, N. Takamure - US Patent 8329599 B2 (2012).

[23] F. Pukelsheim, Optimal Design of experiments, SIAM (editor) (2006).

[24] Thesis of M. Labrot, Low temperature raised source and drain epitaxy for Fully Depleted Silicon on Insulator (FD-SOI) technology (2016).

[25] N. Tsuji, A. Fukazawa, N. Takamure, S. Haukka, A. J. Niskanen, H. S. Park – US Patent 8912101 B2 (2013).

Appendix A: Surface preparation

Type	Products	Process
SC1 (or APM Ammonium Peroxide Mixture)	NH₄OH (ammoniac) then DI water	Removing particles SC1 oxide and desoxidation simultaneously. This has the effect of oxidize the silicon as the basis particles, and then "reject" the particles by electrostatic repulsion during the desoxydation. The effectiveness of SC1 may be increased with the addition of an action Physics: (<i>megasonic or Spray: not used in your case</i>)
SC2 (or <i>dHCl</i> for diluted HCl)	HCl (Hydrochloric acid) then DI water	Removing of metal contamination SC2 dissolved metals. In the case, we will in fact dilute HCL (H ₂ O ₂ not used but single wafer tool).
HF (<i>HF-Last</i>)	HF (Hydrofluoric acid) then DI water then N ₂ -blow dry	Desoxidation Isotropic and selectively. Only the diluted HF (0.25 to 2%) will be used in cleaning recipes: selectively etching the oxide.
RCA	SC1 then SC2	Chemical oxyde
HF-RCA	HF then SC1 then SC2	Process used when the plates must be cleaned and deoxidizing.
SiCoNi [12, 18, 19, 20, 21]	NH₄F plasma	Desoxidation An in-situ dry chemical cleaning technology has been developed and integrated to RT-CVD tool.

Table 8: Clean substrate for contaminations SC1 and SC2 correspond to classical chemical cleans before sample handling.

Appendix B: Atomic Layer Deposition of SiN or SiBCN for spacer

The process to realize a dielectric film having Si-N, Si-C or Si-B bonds on a semi-conductor substrate is based on ALD (Atomic Layer Deposition) [22]. The majority of ALD reactions use two precursors [25]. These precursors react with the surface in a sequential, self-limiting, manner. Through repeated exposures to the different precursors (cycle process), a thin film is deposited. ALD deposition at 450°C-650°C allows a good uniformity, a minimal incorporation of impurities and adequate stoichiometry. The so-obtained silicon nitride is polycrystalline as reported in Ref. 13 and 14.

Appendix C: Design of experiments (DOE) and statistic approach

Our main goals are:

1. A small number of defects
2. A best etching uniformity
3. A SiO₂/Nitride high selectivity

This has been achieved by screening four main experimental parameters

1. NF₃ flow
2. NH₃ flow
3. Etching temperature
4. Sublimation time

For this purpose we use a design of experiments based on 2⁴⁺¹ Fractional factorial design [23]. The so-defined matrix consists in the 11 experiments reported in table 4. Processes 5, 6 and 7 are identical and thus enable to estimate the statistical errors. The other processes of table 4 correspond to nine variants of the initial SiCoNi process. Linear regression models have thus been used to infer the response associated to the screening of the 4 experimental parameters. These fits are obviously relevant only if the variation of the response to a screened-factor is greater than the statistical error bars defined at 1 σ . This is expressed numerically by a quality factor R² close to 1 (R² = 0.998).

Within this scheme (i) the experimental parameters have been optimized, (ii) the statistical errors have been measured. The differences in selectivity (Table 4) or in the total number of defects (Table 5) are thus found to be statistically relevant. For instance the selectivity recorded for processes 9 and 11 table 4 is better than the others when considering the error bars reported in Fig. 7.

Graphical abstract :

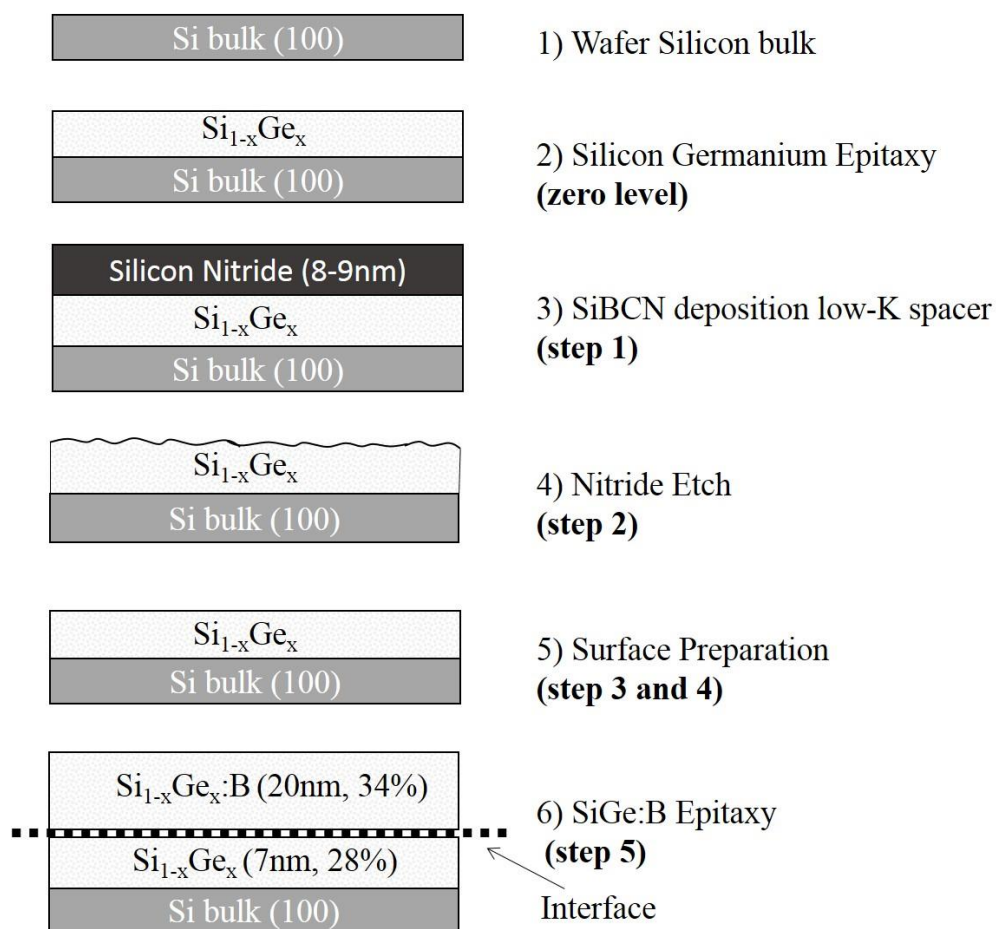


Figure graphical abstract: Description of different SiGe samples (300 mm SOI wafer) under study: 1) initial silicon bulk used as a reference material, 2) SiGe layer grown by epitaxy (channel layer), 3) nitride silicon deposition (low-k dielectric layer), 4) silicon nitride etching, 5) surfaces cleaned by various processes, 6) SiGe:B layer grown by epitaxy (Raised-Source-Drain epitaxy).

Highlights:

- FD-SOI technology requires the use of very thin channel and thus the use of raised sources and drains.
- The quality of the epitaxially grown RSD depends on the surface quality of the channel and thus depends on many technological steps preliminar to the RSD subsequent growth.
- The present report describes how etching and cleaning methods may be improved to reach high quality FD-SOI based CMOS devices.

ACCEPTED MANUSCRIPT