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***Abstract*—This work presents a System-on-Chip designed for Energy-Harvested applications. It embeds an ARM® Cortex®-M0+ microcontroller, 4 KB RAM, 4 KB ROM, an ultra-low power frequency synthesizer, a custom power switch, and a Power Management Unit enabling Active and Sleep modes. The system fabricated in 28 nm FD-SOI technology achieves 2.7 pJ/cycle at 16 MHz during active mode, and the core consumes 4.3 nW during deep sleep mode. The system operates at a fixed voltage of 0.5 V, and can switch from Active and Sleep/Deep Sleep modes, adjusting the frequency from 16 MHz to 8 MHz or 32 kHz in one cycle upon energy availability. By combining frequency/power switching with extra Reverse Body-Biasing the system power consumption is reduced by 53% and 98% in respectively sleep and deep sleep modes.**

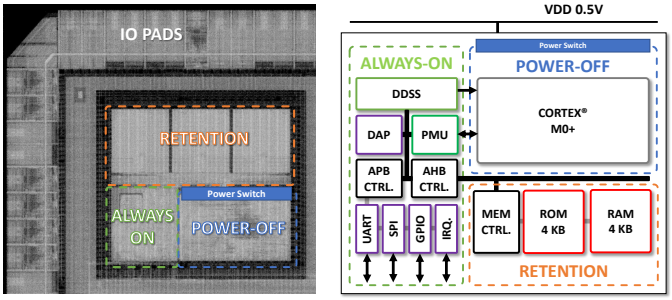


Fig. 1: 28 nm FD-SOI SoC implementation and corresponding block diagram. Active area is 0.073 mm^2.

I. Introduction

Pulsed by the wide variety of low cost, battery-operated and connected applications, Internet-of-Things is considered to be the next decade market with 30.7 billion devices expected in 2020 [1]. Those actual systems' power consumption are in the milliwatt range, hardly sustainable by integrated energy harvesting solutions for autonomous sensor nodes or outdoor monitors [2]. With the advent of new smart objects with perpetual operations, designers and manufacturers must go beyond the Koomey's law which conjectures that the amount of power required for a given computing load will fall by a factor of 2 every 1.5 years. [3]

By enabling efficient low-cost systems, this work aims to push mass market microcontrollers (MCU) down to the microwatts power consumption. The proposed design developed in 28 nm Fully Depleted Silicon-On-Insulator (FD-SOI) technology is based on optimized standard cells and memories in conjunction with design methodology improved for 0.5 V operation with strong tolerance to process variability. The integrated Power Management Unit offers an adaptive power reduction related to the core activity, which helps to achieve 2.7 pJ/cycle ACTIVE and 4.3 nW DEEP SLEEP mode power consumption. This confirms the System-on-Chip's compatibility with power budgets generated by energy-harvesting devices.

In Section II the chosen system architecture and implementation process is presented. The silicon measurements are then presented in Section III. Lastly, an adaptive power reduction analysis is provided based on the core activity in Sec. IV.

II. System Architecture and Implementation

A. System overview

As presented in Fig. 1, the System-on-Chip (SoC) designed is composed of three Ultra-Low Voltage (ULV) power domains:

- An Always-On (AO) integrating a custom Power Management Unit (PMU), a one-cycle switching frequency synthesizer (DDSS), and event triggered peripherals;
- A Power-Off domain that includes an ARM® Cortex®-M0+ core and a custom power switch;
- A retention domain combining 4 KB of RAM and 4 KB of ROM in the form of 2 SRAM banks.

The PMU was designed as a Finite State Machine to enable ACTIVE and Standby Modes (SLEEP and DEEP SLEEP) at very low power cost. The peripherals included are an UART controller, a SPI interface, 10 GPIO ports, a Wake-up Interrupt Controller and the ARM® Debug Access Port. They are memory-mapped to the AHB bus through the APB.

B. Frequency synthesizer operation

The proposed clock generator (Fig. 2) is a custom alternative to PLL which trades-off phase-locking for lower power and area [4]. It operates on a free-running unregulated internal 32-phases oscillator which period T_{RO} is compared with a known 32 kHz reference via a simple counter. That stage output, W, is then used as the input command of a fractional phase-selection divider, providing output periods with $1/32^{nd}$ increments. The oscillator is custom designed, while the rest of the circuit is automatically placed and routed from standard cells. The total clock generator area is 981 μm^2.

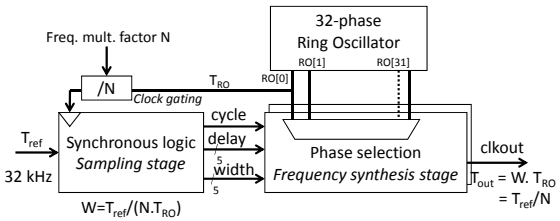


Fig. 2: Block diagram the Direct Digital Sampling and Synthesis (DDSS) clock generator [4].

C. Low energy design considerations

The Cortex®-M0+ minimum active energy operating point (MEP) was extracted using synthesis loops. Various operating conditions and standard cell libraries were explored for $V_{dd} \in [0.45V; 0.9V]$, $F \in [1\,\text{MHz}; 750\,\text{MHz}]$, threshold-voltage $V_{th} \in [Regular; Low]$, and gate-length $L_g \in [30\,\text{nm}; 46\,\text{nm}]$. The MEP was achieved at $0.5\,\text{V}/16\,\text{MHz}$ operating condition, using regular threshold-voltage and 34nm to 46nm gate-length standard cell libraries (*cf.* Fig. 3). Regular-threshold transistors were also selected with regards to the use of Reverse-Body Biasing (RBB) for static power consumption reduction in sleep states.

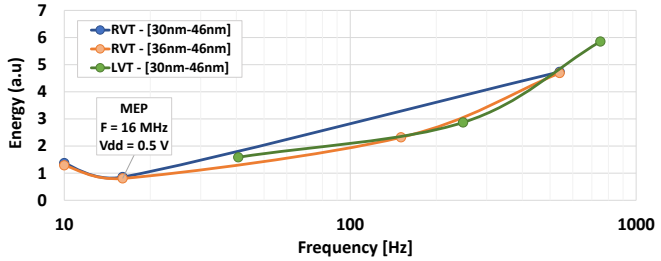


Fig. 3: Subset of Cortex®-M0+ Synthesis loops results for $V_{dd} \in [0.45V; 0.9V]$. Using limited range of gate-lengths and Regular-Threshold Voltage (RVT) standard cell libraries leads to the optimal MEP, with an operating voltage of $0.5\,\text{V}$ and frequency of $16\,\text{MHz}$.

The power switch was strictly designed to minimize the static current consumption. The Cortex®-M0+ was modeled using a current load in the range of $1\,\mu\text{A}$ to $10\,\mu\text{A}$, corresponding to the simulated current profile of the MCU for a given set of programs. The targeted on-resistance (R_{ON}) was defined with a $10\,\text{mV}$ maximum voltage drop target, which induces a limited power impact margin of 2%-4%, that is $R_{ON} \in [1\,\text{k}\Omega; 10\,\text{k}\Omega]$. The switch design is based on distributed LVT pMOS transistors with gate tied to the body, offering fast swing recovery and super shut-off performances (Fig. 4). The restoration time was characterized to remove the need for a feedback controller with acknowledgment, replaced by a hard-coded wait operation. These specifications ensure the minimum power consumption overhead due to the controller area and activity power savings, and the inherent switching time when the SoC goes into DEEP SLEEP. (*cf.* Sec.IV).

The memories used for ROM and RAM are based on 6-transistors bitcells with ultra-low voltage capabilities, enabling operation at $0.5\,\text{V}$ and retention at lower supply values. The full system was implemented with ultra-low voltage corners

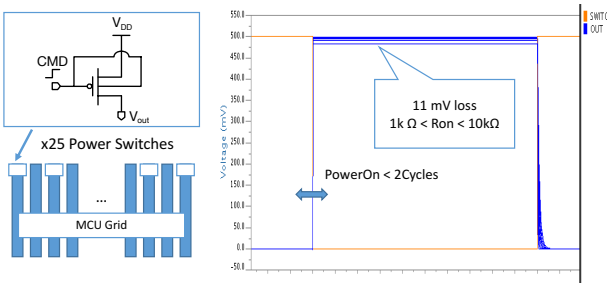


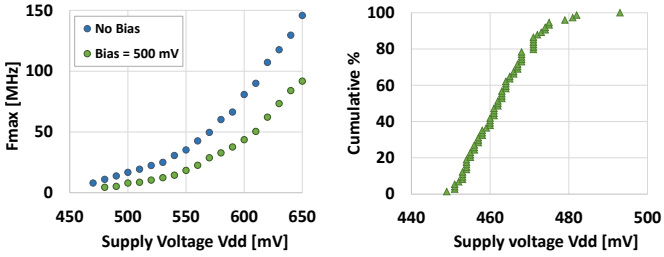
Fig. 4: Distributed power switches using LVT-transistor design and simulated performances at $0.5\,\text{V}$. Total area is $90\,\mu\text{m}^2$.

centered at $0.5\,\text{V}$, with adjusted clock derating, setup and hold uncertainties. The tolerance to variability was improved by checking the hold timing violations at low voltages, fast/slow process and high/low temperatures.

III. Silicon Measurements

A. Benchmarking and measured performances

The system was fabricated in 28nm FD-SOI technology, packaged and measured using a custom development board and a Kintex-7 FPGA from Xilinx. A C-code program running the Dhrystone benchmark, SLEEP and DEEP SLEEP operations is used as software for yield measurements on 80 dies at wafer level, and performances measurements on 5 packaged dies, at 25°C. The speed performance obtained are given in Fig. 5a for $V_{dd} \in [0.45\,\text{V}; 0.65\,\text{V}]$. The mean clock frequency goes from $10\,\text{MHz}$ at $0.47\,\text{V}$ to $150\,\text{MHz}$ at $0.65\,\text{V}$ with the targeted $16\,\text{MHz}$ at $0.5\,\text{V}$. The F_{max} associated to a RBB bias voltage of $500\,\text{mV}$ is also plotted. Its utilization in SLEEP and DEEP SLEEP modes is scheduled for static power consumption reduction (Sec. IV).



(a) F_{max} VS. V_{dd}. (b) % of working parts VS. V_{dd}.

Fig. 5: Measured silicon performances as function of V_{dd}.

Regarding the yield, the cumulative percentage of working parts from $0.45\,\text{V}$ to $0.5\,\text{V}$ is reported in Fig. 5b, as extracted from the wafer. These silicon results show that the reference processor can be supplied down to $0.48\,\text{V}$, within a variability window of less than 2%.

B. Power evaluation

The power contribution of each parts of the system was measured separately at $0.5\,\text{V}/16\,\text{MHz}$, plotted in Fig. 6 and the figures associated reported in the first row of Tab. I. The total energy consumption when the system is running is $2.67\,\text{pJ/cycle}$. The total power consumption due to the static current is $1.5\,\mu\text{W}$, dominated by the M0+ core.

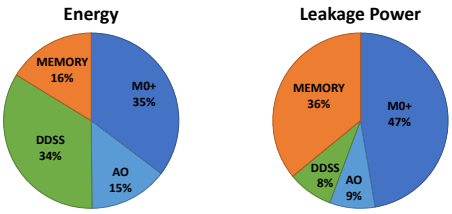


Fig. 6: Pie chart of the energy/cycle (left) and the leakage power (right) SoC's repartition.

IV. Cortex® M0+ with adaptive power reduction

A. Available low power modes

The ultra-low power application oriented Cortex®-M0+ processor is a 32-bit ARMv6 architecture with a two-stage pipeline for improved response time and efficiency. Thus, it achieves lower power/higher performances when compared to the previous M0 core [5].

Architecturally, two sleep modes are proposed: normal SLEEP and DEEP SLEEP. In our implementation, the SLEEP behavior is defined by the clock gating of the M0+ core whereas the DEEP SLEEP enables the use of the power switch on the Power-Off domain. Based on these sleep mode features, a PMU was designed and merged with a Wake-up Interrupt Controller (WIC) as additional hardware level to enable mode transitions. With this architecture the SoC user has the opportunity – depending on their application requirements – to clock gate or power down the microcontroller and wake up on certain hardware events.

B. Resulting power savings

Table I demonstrates the leverage offered by the M0+ power modes combined with the PMU to reduce power consumption of the system. All measurements were performed at 0.5 V/16 MHz. Switching from ACTIVE to SLEEP power mode leads to reduce the core power consumption from 15.1 µW to 1.96 µW, reaching its lowest value of 4.3 nW in DEEP SLEEP.

TABLE I: Energy/cycle and power breakdown

State	M0+	Always-ON	DDSS	Memory	Units
ACTIVE	**0.94**	0.39	0.89	0.44	pJ/c.
	15.1	6.23	14.5	6.96	µW
IDLE[1]	0.86	0.38	0.89	0.25	pJ/c.
	13.7	6.23	14.5	4.02	µW
SLEEP	0.12	0.22	0.89	0.03	pJ/c.
	1.96	3.59	14.5	0.53	µW
DEEP SLEEP	$2.7e^{-4}$	0.21	0.89	0.03	pJ/c.
	4.3 nW	3.49	14.5	0.54	µW

[1] IDLE given as the worst waiting option corresponding to active polling.

In low power modes, the fastest clock frequency is no longer necessary. Consequently by switching in one cycle the DDSS clock from 16 MHz to 8 MHz the power consumption of the Always-On (SoC) is reduced by 48% (13%). For further power saving, the DDSS is disabled in DEEP SLEEP and the 32 kHz reference clock is used. As reported in Fig. 7 this last technique decreases the AO/SoC power consumption by 95%.

Subsequently, trimming the SoC frequency offers room for Reverse Body-Biasing (RBB) usage leading to a SoC

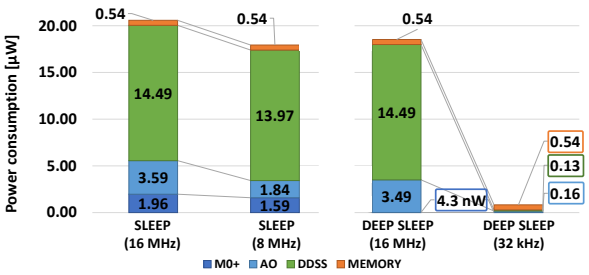


Fig. 7: Influence of frequency scaling on the power consumption in SLEEP (left) and DEEPSLEEP (right) modes.

static current consumption reduction of 31% and 12.5% in respectively SLEEP and DEEP SLEEP as explained in Fig. 8.

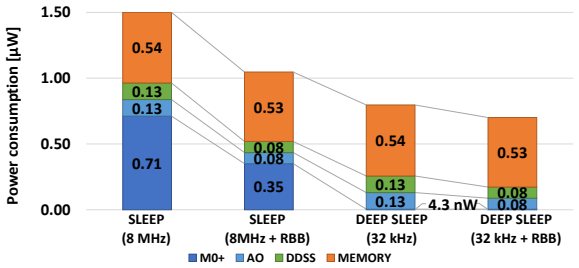


Fig. 8: Reduction of the leakage power using RBB.

By combining together, all these power saving approaches, we induced a power breakdown from ACTIVE to SLEEP with frequency scaling & RBB and DEEP SLEEP with power gating, frequency scaling & RBB of respectively 53% and 98%. This leads to a total power consumption of the SoC of 0.7 µW in DEEP SLEEP mode (*cf.* Fig 9).

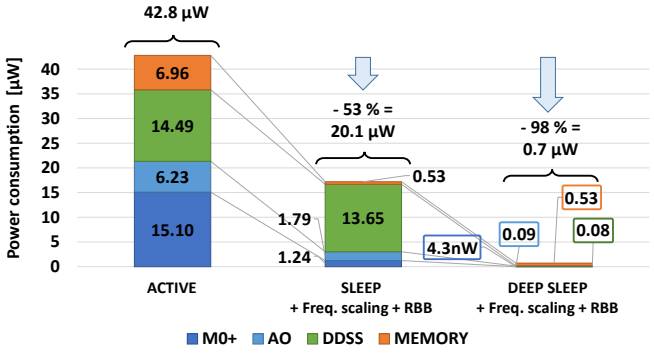


Fig. 9: Total power breakdown of the SoC.

Lastly, the power modes selected and the associated actions are summarized in Table II.

TABLE II: Summary of power modes available

State option	ACTIVE	SLEEP +Freq. scal. +RBB	DEEP SLEEP +Freq. scal. +RBB
AO clock	16 MHz	8 MHz	32 kHz
DDSS	ON	ON	OFF
M0+ clock	16 MHz	Gated	Gated
Power switch	ON	ON	OFF
Body bias	0 V	RBB 0.5 V	RBB 0.5 V

C. Adaptive mode selection according to time spent in a mode

The time required to switch the processor between states results in longer response latency and consume a fair amount of energy. The most energy-efficient SoC inactive state depends of these power and timing penalties. Hence, to select the lowest power mode for a given timeout, it is necessary to evaluate the energy overhead due to these transitions.

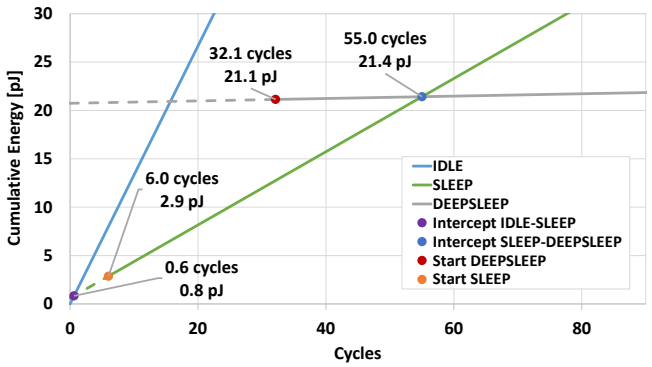


Fig. 10: Evolution of the energy consumption in pJ for selected power state.

Fig. 10 gives an insight into power modes switching and the associated figures. Using these performance measurements, the designer can select the best mode according to the SoC activity. The IDLE state is given as the worst power saving mode. It ideally starts in 0 clock cycles and corresponds to an active polling mode of the MCU.

The switching time from ACTIVE to SLEEP or DEEP SLEEP and the associated energy are defined by design. They have been validated using RTL and Prime Time power simulations. This time results in a minimum number of cycle and energy reported in Fig. 10 using the red and orange dots, respectively for SLEEP and DEEP SLEEP modes. The slopes are given by the energy/cycle associated to each mode. Finally, the blue and purple dots define the time when mode switching is beneficial in terms of energy.

Hence, for energy driven applications, the gains of entering the power-off modes is benchmarked: the SLEEP state can directly be selected. Indeed only 0.6 ($\leq$1) cycle of overhead is reported. However, for sleep time over 55 cycles the DEEP SLEEP should be triggered because it leads to the lowest SoC energy mode.

In the case of duty cycled core operations, the sum of the times spent in ACTIVE mode T_{ON} and sleep mode T_{OFF} is constant. Knowing T_{ON} through a simple counter gives us T_{OFF} and therefore the best sleep mode can be chosen.

D. Detailed comparison with the state of the art

The performances of the system is compared with the latest state of the art 32-bit microcontrollers in Table III. This work combines a low power consumption SoC with excellent energy/cycle associated with a PMU allowing efficient dynamic power mode selection.

V. Conclusion

This research presents a System-on-Chip fabricated in 28nm FD-SOI, optimized for energy-harvested applications and offering mass market MCU with very high efficiency: 2.7 pJ/cycle at 0.5 V/16 MHz in ACTIVE mode, and 4.3 nW MCU in DEEP SLEEP mode. A frequency synthesizer enabling one-cycle frequency scaling, a dedicated power switch, and a PMU offering efficient mode switching lead to reduce the SoC power consumption down to 0.7 µW. The system power signatures fit in the energy-harvesting ~100 µW power budget, demonstrating autonomous system capabilities [2].

Acknowledgements

The authors would like to thank their colleagues David Bonciani and Janit Kumar, Manohara Mr and Amit Patel for wafer testing and testing board design respectively.

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TABLE III: Summary of the achieve performances and state of the art comparison

Feature	**This work**	ESSCIRC'16 [6]	JSSCC'16 [7]	ISSCC'15 [8]	ESSCIRC'15 [9]
Technology	**28 nm FDSOI**	40 nm CMOS	65 nm CMOS	180 nm CMOS	28 nm FDSOI
Core	**ARM® Cortex®-M0+**	ARM® Cortex®-M0	ARM® Cortex®-M0+	ARM® Cortex®-M0+	ARM® Cortex®-M4
Memory	**4 KB ROM** **4 KB SRAM**	256 KB 4 KB SRAM	2 KB ROM, 16 KB SRAM 8 KB ULV SRAM	256 B	16 KB SRAM
Total Area [mm^2]	**0.073**	2.55	3.76	2.04	0.15
$V_{dd,MEP}$	**0.5 V**	0.44 V	0.39 V	0.55 V	0.5 V
F_{max} @MEP	**16 MHz**	31.2 MHz	688 kHz	7 Hz	45 MHz
DEEP SLEEP power	**4.3 nW**	–	–	–	–
E/Cycle @F_{max} [pJ]	**0.94 (core)** **2.67 (total)**	16.07 (core) 100.34 (total)	– 11.7 (total)	– 92.04 (total)	– 8.9 (total)