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# A 0.40 pJ/cycle 981 $\mu\text{m}^2$ Voltage Scalable Digital Frequency Generator for SoC Clocking

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**Abstract**—This work presents a compact voltage and frequency scalable clock generator for low-power digital SoC clocking. Named Direct Digital Sampling and Synthesis (DDSS), the open-loop generator implemented in 28 nm FD-SOI operates from 0.45 V to 1.1 V with measured jitter from 2.0% to 5.1% UI. Its low power consumption of 0.40 pJ/cycle at 57 MHz 0.5 V combined with the ability to perform fast frequency changes makes this circuit an alternative to PLLs for fast Dynamic Voltage and Frequency Scaling (DVFS) strategies in low power SoCs.

## I. INTRODUCTION

The last decade has seen a trend in taking advantage of digital logic downscaling to port analog building blocks into digital designs. This has enabled area savings and voltage downscaling for elements such as power monitors, temperature sensors as well as Phase Locked Loops (PLLs) [1]–[5]. The All Digital PLLs now replace the traditional LC oscillators and charge pumps with ring oscillators and digital loop filters.

These circuits offer better area and power performance, at the expense of slightly higher jitter values, which is less critical for clocking than for RF applications. However, due to their closed loop nature, the digital PLLs face the same lock time restrictions as their analog counterparts. Some instant switching strategies added to the PLLs come at the price of added area and power consumption [3].

Moreover, power management strategies rely heavily on fine grain frequency scaling [6]. This fine granularity applies both in space and time, requiring a clock generator with low area and instant switching capability respectively. To limit its power overhead, the clock generator also needs a low leakage current, in clock gating mode, and a wide voltage scalability with output frequency matching that of the digital logic it clocks.

The open-loop principle of Direct Digital Sampling and Synthesis (DDSS) [7] offers an alternative to PLLs, trading off the phase locking for instant switching. The previously published DDSS, however, suffered from limited voltage and frequency scalability (0.6 V minimum voltage, 574 MHz maximum frequency at 0.9 V), as well as a complicated calibration mechanism, limiting its practical use.

The proposed design, implemented in 28nm FD-SOI, improves on the DDSS principle by using a phase selection approach to the fractional division unit, rather than delay lines. Compared to [7], this method allows for a simpler calibration-free design, offering a 14x reduction in area down to 981  $\mu\text{m}^2$ , as well as extended voltage operating range (down to 0.45 V), 6.5x reduction in power consumption at Vmin and a maximum frequency on par with digital clocking requirements (879 MHz vs 574 MHz at 0.9 V). This makes the phase selection based

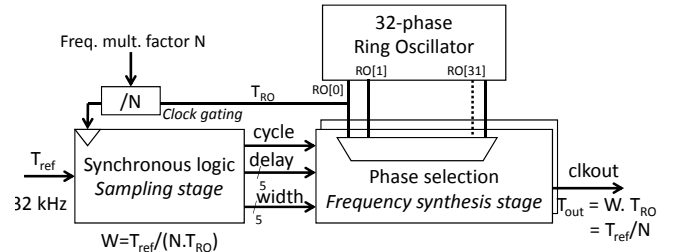


Fig. 1. Principle of operation of the DDSS clock generator.

DDSS a good candidate for low power voltage scalable Globally Asynchronous, Locally Synchronous (GALS) SoCs.

## II. CIRCUIT ARCHITECTURE

### A. Direct Digital Sampling and Synthesis

Fig. 1 illustrates the phase selection principle of operation of the phase-selection based DDSS. A low frequency clock reference of period  $T_{ref}$  is provided (for example from an off-chip quartz). First, in the *sampling stage*, the reference frequency is compared with the period  $T_{RO}$  of an internal free-running ring oscillator via a simple counter, which produces a digital output  $W$  proportional to  $T_{ref}/T_{RO}$ . Thanks to a configurable clock gating, the first stage counter is incremented by one every  $N$  cycles of  $T_{RO}$ , resulting in  $W = T_{ref}/(N \cdot T_{RO})$ .

Then, in the *synthesis stage*, a phase selector operates the fractional frequency division of the RO by a programmable factor proportional to the first stage output  $W$ , ie  $T_{out} = T_{RO}/W = T_{ref}/N$ . By using the same RO reference for the sampling and synthesis stages, this feed-forward design guarantees that the output frequency is  $N$  times that of the reference, independently of the exact RO frequency.

The feed-forward topology also provides an immediate change in  $W$  and  $T_{out}$  as soon as  $N$  or  $T_{ref}$  are changed, without need for a re-locking time.

Contrary to delay line types of fractional division [3], [7], the phase selection method does not require any specific calibration, as the sum of the 32 phases delay is by construction equal to one period  $T_{RO}$  of the ring oscillator. The only timing constraint is that  $T_{RO}$  must be larger than the setup time of the synchronous logic stage. But as this logic is very simple this setup constraint is low (0.61 ns at 0.9 V) and can be safely margined.

Last, thanks to a selection of both the rising and falling edge of the generated clock, the width of the output pulse and hence its duty cycle can be controlled.

### B. Oscillator design

Fig. 2 presents the schematics and layout of the 32-phase ring oscillator. It is based on a conventional cross coupled

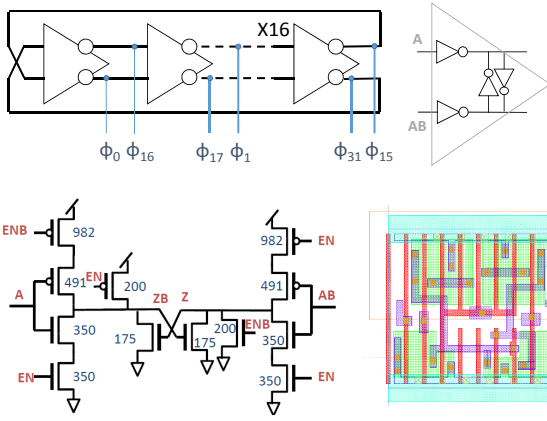


Fig. 2. Top: principle of the 32-phase RO. Bottom: schematics and layout of a differential inverter stage

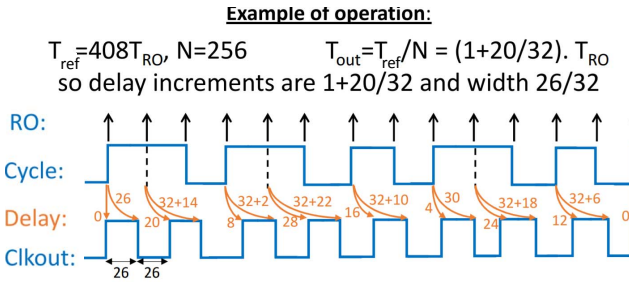


Fig. 3. Example of the DDSS operation.

inverter pair topology. The transistor-level design is optimized as the inverter pair is reduced to minimum sized NMOS only to reduce area and power. An enable command is also added at each stage to enable ring gating for power savings in idle mode. This command is added on each of the 16 stages to avoid phase imbalance. Last, the design is laid out in order to allow abutting between stages and with standard cell logic without area overhead.

### C. Phase selection principle

Fig. 3 illustrates the general principle, with the commands cycle and delay sent to the phase selection block. On each cycle the rising and falling edge delay values are incremented by one step ( $20/32$  in the example). When the increment overflows, the cycle command is set to 0 for one cycle and no pulse is processed.

Fig. 4 presents the details of the phase selection operation. The general principle, illustrated in sub-figure 4.a) consists in using a flip-flop to propagate a selected phase at its rising edge. The conceptual timing of the selection, presented in sub-figure 4.b), is first to set the phase multiplexer selection, then to enable the edge capture by setting the "window" D input of the flip-flop to 1. However, as illustrated on the timing diagram, some margin must be set between the selection: (1) for multiplexer setting before the window is enabled, (2) and (3) are the timings the window needs to be enabled before and after the desired edge is selected and (4) for disabling the window before the multiplexer command is changed.

Because of these constraints, the phase selection cannot be performed in a single cycle: the full window has to cover the phases  $\phi_0$  to  $\phi_{31}$  plus the margins (1-4). For this reason, two Phase Selection Units (PSUs) run in parallel, each operating over 2 cycles. The first half of the first cycle is used to

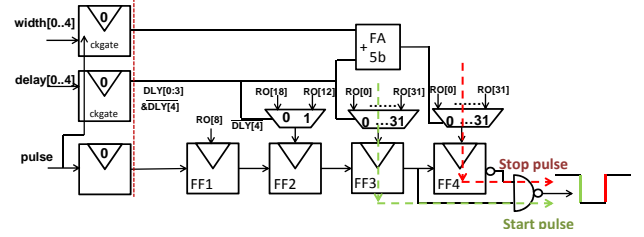
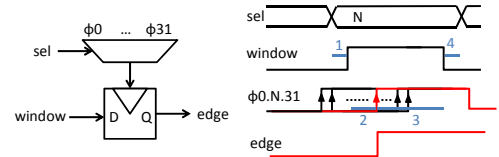


Fig. 4. a) Top left, principle of flop based phase selection, b) Top-right resulting timing constraints c) bottom, full schematic of a Phase Selection Unit (PSU).

guarantee constraints (1) and (2), one cycle for the actual phase selection and another half cycle for constraints (3) and (4). The sub-figure 4.c) presents the details at gate level of the implementation. The first two flip-flops FF1 and FF2 guarantee the margin (1) and (2), while the FF3 selects the rising edge and FF4 the falling edge. Moreover, the only cells affecting the output jitter are the 32:1 MUX and the FF3, which limits mismatch impact of the two parallel PSUs. This design is very compact and easy to implement, requiring only 44 standard cells per PSU.

### D. Digital flow and simulations

The highly digital and very compact nature of the DDSS take benefit of the digital flow for quick design iterations, to explore different design strategies and cells sizings as well as timing verification and simulations. The trade-off being that the automated P&R does not ideally match timing between paths, causing added deterministic jitter.

The size (13k transistors total) and digital behavior of the circuit makes full SPICE simulations on the extracted netlist possible. This allows for simulation of the estimated output deterministic jitter due to delay mismatch between the gates.

Fig. 5 shows the results of the simulation. In green cross the nominal run across three corners shows the effect of P&R mismatch only, while the box plot shows the spread of 25 Monte Carlo runs. This simulation predicts the level of jitter expected and demonstrates that at low voltage its dominant contributor is the random variation rather than P&R mismatch, which validates the digital flow approach.

## III. MEASURED PERFORMANCES

### A. Testchip implementation

Fig. 6 presents the full test vehicle view, details of the DDSS layout and test harness. 16 chips have been fabricated, packaged and measured. The testchip integrates frequency dividers to allow validation of functionality even at GHz frequency range where standard digital IOs cannot transmit the generated clock off chip directly. The circuit is designed in a 28nm FD-SOI Regular Voltage Threshold (RVT) process to minimize leakage in idle mode for low power applications. The total DDSS area is  $981 \mu m^2$  and can be placed inside of digital logic with no guard area overhead.

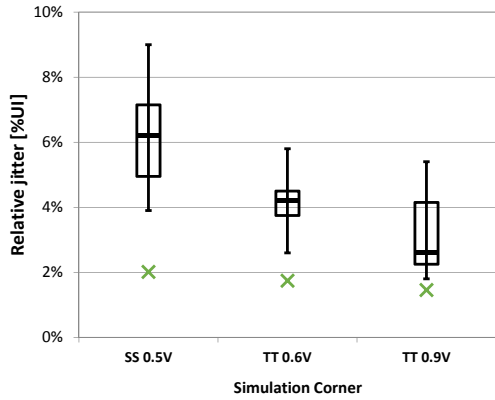


Fig. 5. Extracted Spice simulations of the full design across corners. Green cross: nominal run, box plot: result of 25 Monte Carlo runs.

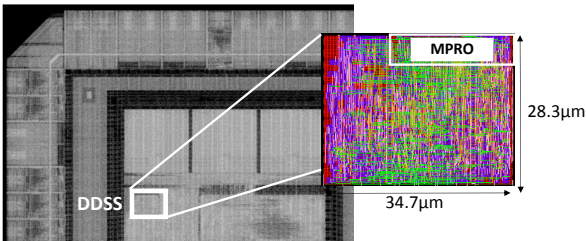


Fig. 6. View of the test chip and DDSS layout.

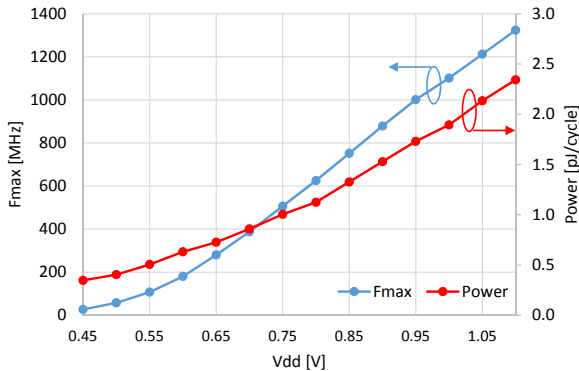


Fig. 7. Maximum output frequency and energy consumption of the clock across 0.45-1.1V range. Median values at room temperature across 16 dice.

### B. Maximum frequency and power

Fig. 7 shows the measured maximum generated frequency and power consumption at  $F_{max}$  of the 16 chips across 0.45 V to 1.1 V supply. The circuit achieves an energy efficiency of 0.45 pJ/cycle at 57 MHz 0.5 V and 1.53 pJ/cycle at 879 MHz 1 V.

Table I (median value measured across 16 dice) shows the DDSS can be Reverse Body Biased (RBB) at the same time as the core when it is power gated for 6x to 11x leakage reduction, down to 10 nW at 0.5 V 1.5 V RBB, enabling Internet of Things type duty-cycled operations.

### C. Duty cycle control

As described previously, the phase selection approach makes it possible to control the pulse width. This is implemented in practice by 7 settings, the first 4 control the width from 1/8th to 4/8th, while the last 3 invert the output of the first

TABLE I. LEAKAGE POWER IN POWER OFF MODE AT 0.5V AND 1V SUPPLY AND DIFFERENT BIAS LEVELS.

Vdd \ Vbb	no BB	0.5 V RBB	1 V RBB	1.5 V RBB
0.5 V	0.11 $\mu$ W	0.04 $\mu$ W	0.02 $\mu$ W	0.01 $\mu$ W
1 V	0.60 $\mu$ W	0.25 $\mu$ W	0.16 $\mu$ W	0.10 $\mu$ W

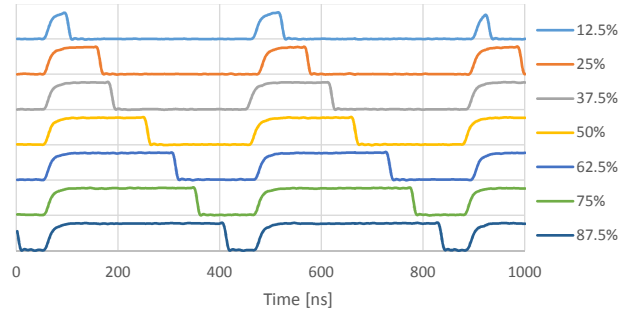


Fig. 8. Measured clock output with the seven available duty cycle settings.

3. This sets 7 settings between 1/8th to 7/8th. This feature is illustrated in the measured data of fig. 8. This feature is useful to offset clock tree unbalance at lower voltages and can be used in low power pulse based latch logic [8].

### D. Jitter measurement

First, it is important to note that the jitter constraints are different for SoC clocking than for RF or data recovery applications. The relative peak to peak period jitter is the main metric and directly translates to a frequency penalty, or extra margining in the digital logic the DDSS clocks. For example a 6% UI jitter corresponds to only a 3%  $F_{max}$  degradation in the clocked logic.

Fig. 9 presents the rms and peak-to-peak jitter measurements at 0.5 V across the 16 dice, as well as a capture of a jitter histogram, illustrating the superposition of the deterministic component, from phase selection paths mismatch, with the random jitter from supply and components noise. As the deterministic jitter is dependent on the phase increment values, the values are measured for the 16 dice and two different output frequencies (20 MHz and 35 MHz) to demonstrate measurements are not made on a best case. The median measured peak-to-peak jitter value is 1.47 ns and 2.01 ns at 35 MHz and 20 MHz, ie 5.1% and 4.0% UI respectively.

Due to IO bandwidth, the jitter at 0.9 V is measured at 100 MHz. Median value of pk-pk and RMS jitter is 167 ps and 20.7 ps, ie 1.7% UI and 0.21% UI respectively.

### E. SoC level performance

This jitter performance has to be put in perspective with the full SoC power budget. As an illustration, the test-chip also includes a low power ARM M0+ core [9] operating at the same voltage and clocked by the DDSS. On a Dhrystone testbench the M0+ consumes 0.94 pJ/cycle at 0.5 V. Hence, when compared to an ideal clock, the DDSS with a 5.1% UI jitter requires an increase in frequency margin of 2.6%. From measured data, this corresponds to a 1.6 mV increase in core voltage for margining, which in turn increases the core energy by only +1.1% ie. by 0.01 pJ/cycle. So, for low power cores, the benefit of the energy efficiency improvement in the clock generator far outweighs the penalty in jitter performance compared to some conventional PLLs [3], [5].

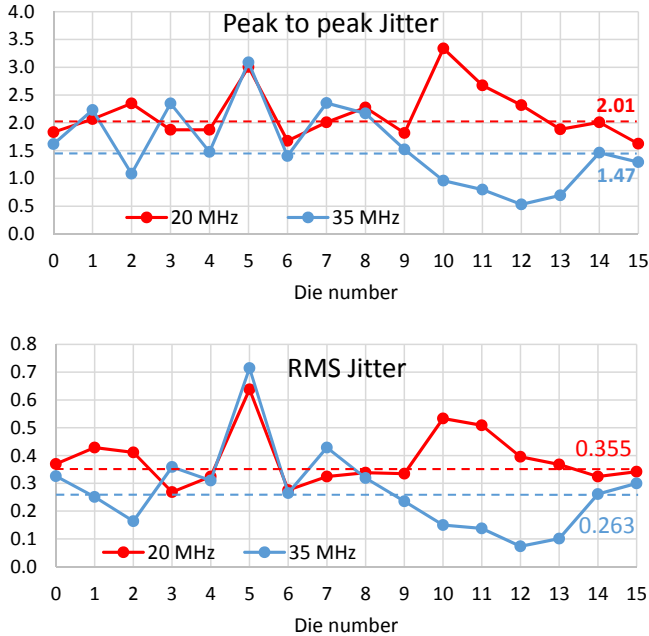
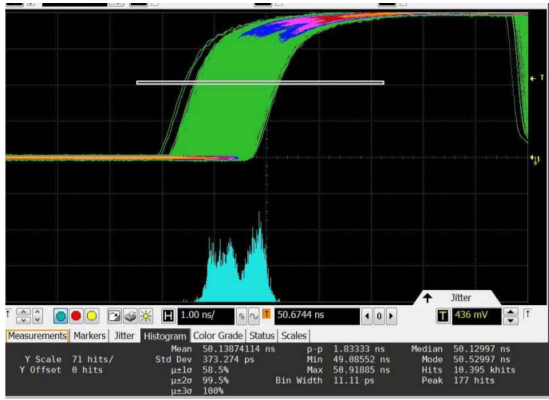


Fig. 9. Top: details of the measurements on die 0 at 20MHz. Bottom: Jitter measurements on 16 dice at 0.5V with 20MHz and 35MHz output frequency.

#### F. Comparison with the state of the art

Table II summarizes the performance of the proposed DDSS clock generators compared with previous DDSS and state of the art PLLs. This work combines a wide voltage range with frequencies compatible with digital logic clocking (unlike [2]), the best reported area and an excellent maximum energy efficiency of 0.40 pJ/cycle.

TABLE II. COMPARISON OF THE PROPOSED ARCHITECTURE WITH STATE OF THE ART ALL-DIGITAL CLOCK MULTIPLIERS

	This work		ISCAS 2016 [7]		TCAS 2016 [1]		JSSC 2013 [2]		ISSCC 2014 [3]	ISCAS 2014 [4]		JSSC 2015 [5]	
Technology	28nm FD-SOI RVT		28nm FD-SOI LVT		90nm CMOS		90nm CMOS		65nm CMOS	90nm CMOS		65nm CMOS	
Design	Open-loop multi-phase		Open-loop DL		All-digital PLL								
Instant switching	Yes		Yes		2 cycles		No		Yes	7 cycles		No	
Automated P&R	Yes (except RO)		Yes		No		No		No	No		Yes	
Duty-cycle control	Yes		No		No		No		No	No		No	
Supply [V]	0.45-1.1		0.6-1.2		0.52-1		0.25-0.5		0.9	1.2		0.8	
Area [ $\mu\text{m}^2$ ]	981		14,000		65,000		57,000		120,000	64,600		6,600	
Normalized area	1		14.3		6.4		5.6		22.7	6.3		1.2	
	0.5V		0.9V		0.52V		1V		0.25V	0.5V			
Fmax [MHz]	57		879		93		574		120	600		48	
E/cycle [pJ]	0.40		1.53		1.53		4.75		0.31	8.4		0.062	
Jitter pk-pk [% UI]	5.1		1.7 <sup>b</sup>		2.7		5.6 <sup>a</sup>		1.9 <sup>c</sup>	4.9 <sup>c</sup>		3.0	

<sup>a</sup> Simulated value.

<sup>b</sup> At 100 MHz.

<sup>c</sup> Only rms value reported, peak to peak jitter estimated as 6 times the rms.

## IV. CONCLUSION

This paper proposes a novel implementation of the Direct Digital Sampling and Synthesis (DDSS) frequency generation circuit. This all-digital approach, compared to conventional PLLs, offers instant frequency scaling. By using a phase selection approach, this circuit offers an extremely compact implementation ( $981 \mu\text{m}^2$ ) and low power across a full 0.45 V–1.1 V operating range, with 0.40 pJ/cycle at 0.5 V. This combined with its satisfying jitter performance (5.1% UI at 35 MHz 0.5 V) demonstrates the possibility for important system-level energy savings from single clock domain ultra low-power systems to large GALs SoCs.

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