SEU Sensitivity of Junctionless SOI MOSFETs-based 6T SRAM Cells Investigated by 3D TCAD Simulation

Daniela Munteanu, Jean-Luc Autran

HAL Id: hal-02100273

https://amu.hal.science/hal-02100273

Submitted on 15 Apr 2019

SEU Sensitivity of Junctionless SOI MOSFETs-based 6T SRAM Cells Investigated by 3D TCAD Simulation

D. Munteanu[a], J.L. Autran[a,*]

[a] *Aix-Marseille Univ, CNRS, Univ Toulon, IM2NP (UMR 7334), Faculté des Sciences – Service 142, Avenue Escadrille Normandie Niémen, F-13397 Marseille Cedex 20, France*

Abstract

The Junctionless (JL) Single-Gate SOI (JL-SOI) technology is potentially interesting for future ultra-scaled devices, due to a simplified technological process and reduced leakage currents. In this work, we investigate, for the first time, the radiation sensitivity of JL-SOI MOSFETs and 6T SRAM cells. A detailed comparison with JL Double-Gate (JL-DG), inversion-mode (IM) SOI (IM-SOI), and IM-DG MOSFETs has been performed. 3-D simulations indicate that JL-SOI MOSFETs and SRAM cells are naturally less immune to radiation than the other structures.

Corresponding author.
jean-luc.autran@univ-amu.fr
Tel: + 33 (0)413 594 627; Fax: +33 (0)491 288 531

SEU Sensitivity of Junctionless SOI MOSFETs-based 6T SRAM Cells Investigated by 3D TCAD Simulation

D. Munteanu[a], J.L. Autran[a, *]

1. Introduction

As the MOSFET is scaling down, the sensitivity of integrated circuits to radiation coming from space or present in the terrestrial environment has been found to seriously increase [1]. For ultra-scaled devices entering in the area of nanoelectronics, natural radiation at ground level is presently inducing one of the highest failure rates of all reliability concerns [2]. In particular, ultra-scaled memory integrated circuits have been found to be more sensitive to single-event-upset (SEU) induced by ionizing particles.

To meet the roadmap requirements in the nanometre scale, several promising technological solutions have been proposed, such as the Fully-depleted Single-Gate SOI technologies (FDSOI) fabricated with ultra-thin silicon bodies. FDSOI devices show enhanced performances in terms of channel potential control, reducing short-channel (SCE) and floating body effects (FBE). A new concept of MOSFET without junctions, called junctionless (JL) MOSFET has been proposed these last years and experimentally validated [3,4,5]. A JL MOSFET designed with a single-gate SOI structure (JL-SOI, Fig. 1a) is an SOI transistor with the same type of semiconductor throughout the entire silicon film, including the source, channel and drain regions. JL-SOI devices present a real advantage since their fabrication process is simplified compared to the conventional process: there are no doping gradients in the device [5] and no semiconductor-type inversion. In addition, the junction leakage currents are totally suppressed and the off-state current (I_{OFF}) is uniquely controlled by the gate, which could be very attractive for ultra-short devices.

From a radiation-sensitivity point of view, the high doping level in the film of a JL MOSFET could have a negative impact on its immunity to single events,

* Corresponding author. jean-luc.autran@univ-amu.fr
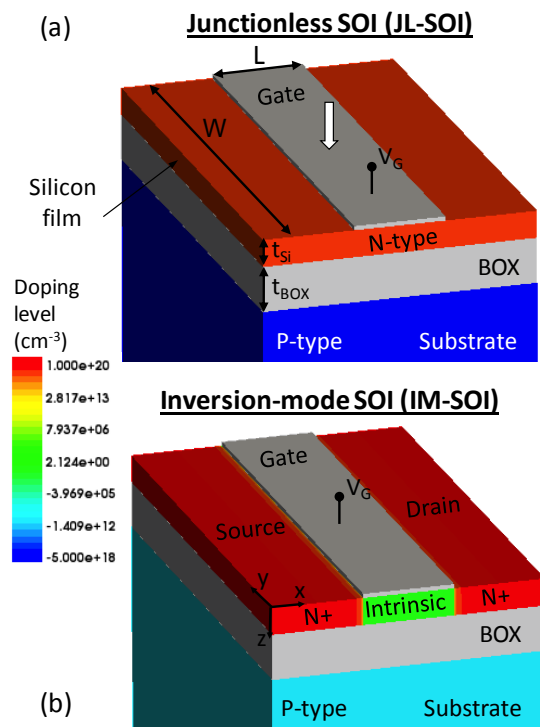Tel: + 33 (0)413 594 627; Fax: +33 (0)491 288 531

Fig. 1. Schematic description of the simulated JL-SOI (a) and IM-SOI (b) MOSFETs. For a better view spacers and isolation oxides are not shown.

because floating body effects are expected to be strong. This was confirmed by our previous works [6,7] concerning the radiation-induced transient behaviour of JL Double-Gate (JL-DG) MOSFETs. In the present work, we investigate, for the first time, the radiation sensitivity of JL-SOI, in terms of bipolar gain of individual devices and SEU sensitivity of six-transistor (6T) SRAM cells. A detailed comparison with JL-DG, inversion-mode (IM) FDSOI (IM-SOI), and inversion-mode double-gate (IM-DG) MOSFETs and 6T SRAM cells has been also performed.

2. Simulation details

Figure 1 shows schematic 3-D descriptions of the simulated JL-SOI and IM-SOI devices. JL-SOI devices are designed with 100 nm gate width, 6 nm-thick silicon film and 0.9 nm-thick gate oxide. The entire silicon film is uniformly n-type doped at 10^{19} cm^{-3}; there are no highly-doped source/drain regions. A 10 nm-thick buried oxide (BOX) and a thick silicon substrate doped at 5×10^{18} cm^{-3} have been also considered. IM-SOI (Fig. 1b) devices have an intrinsic channel; source and drain regions are highly n-type doped and the doping profile in these regions is uniform. The silicon film, BOX and silicon substrate of IM-SOI have the same geometrical parameters as those of JL-SOI. The silicon substrate is lowly-doped at 10^{16} cm^{-3}. IM-DG and JL-DG structures are based on real devices reported in [8]. The silicon film of IM-DG and JL-DG has the same geometrical parameters and doping profiles as the silicon film of IM-SOI and JL-SOI, respectively, with the notable exception that two gates connected together control the channel potential. These four different structures have been first simulated with 20 nm-channel length, considering a power supply voltage of 0.75 V. These devices have been calibrated on the ITRS LP; to facilitate the comparison, the gates work functions have been finely tuned to achieve the same I_{OFF} for all devices. Secondly, additional simulations have been carried out for other channel lengths and power supply voltages.

3-D numerical simulations have been performed with the DESSIS device simulator from Synopsis Inc. [9]. The main models used in simulation are: SRH and Auger recombination models, Fermi-Dirac carrier statistics, hydrodynamic model for the carrier transport, mobility model including the dependence on the carrier energy, lattice temperature and doping level and impact ionization model depending on carrier energy. The ion strike was simulated using the DESSIS HeavyIon module [9]. The electron-hole pair column created in the device by the ion strike is modeled using a carrier-generation function which has a Gaussian radial distribution with a characteristic radius of 20 nm and a Gaussian time distribution, centered on 10 ps and having a characteristic width of 2 ps.

3. Static characteristics of individual devices

The simulated steady-state drain current characteristics of JL-SOI, IM-SOI, JL-DG and IM-DG are plotted in Fig. 2. The devices have the same
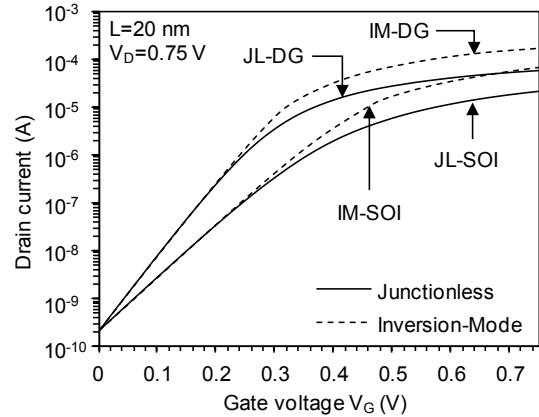

Fig. 2. Drain current as a function of gate voltage for JL-SOI, IM-SOI, JL-DG and IM-DG. The gate workfunction of each device has been tuned to obtain the same I_{OFF}.

off-state current, but different subthreshold swings and on-state currents. While double-gate devices (both JL-DG and IM-DG) have near ideal subthreshold swings (65 mV/dec), SOI devices have a much higher subthreshold swing (90 mV/dec) because the single-gate configuration reduces the control by the gate of the channel potential and increases the parasitic short-channel effects compared to a double-gate configuration. JL-SOI has the lowest on-state current because the highly-doped silicon film degrades the mobility. The highest on-state current is obtained in IM-DG, due to the combination of a double-gate structure and an intrinsic channel; this structure has the advantage to maximize the carrier mobility.

4. Single-event transients

4.1. Drain current, collected charge and bipolar gain

Figure 3 shows the drain current transient resulting from an ion hit in the channel center of JL-SOI and IM-SOI devices. The time variations of the collected charge are also reported on the same figure. The drain current transient peak and width are higher in JL-SOI than in IM-SOI, probably due to a higher bipolar gain. In addition, the drain current decay after the ion strike is slower for JL-SOI than for IM-SOI. The reason is that the floating body effects are more important in JL-SOI than in IM-SOI, due to the high doping level in the JL-SOI film (since the device channel is intrinsic in IM-SOI). The collected charge and the bipolar amplification as function of the ion LET are plotted in Figs. 4a and 4b. The values obtained in [6] for JL-DG and IM-DG devices are also reported in these figures
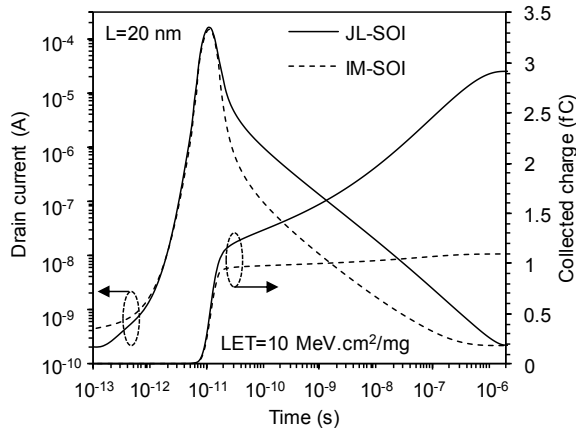
Fig. 3. Drain current transient and collected charge in JL-SOI and IM-SOI for an ion hit in the channel center.
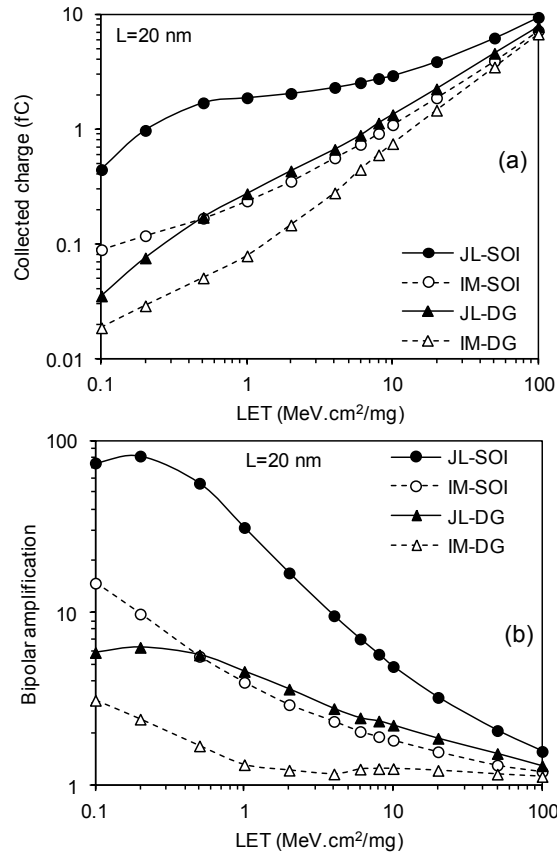

Fig. 4. Collected charge and bipolar amplification as function of LET in JL-SOI and IM-SOI MOSFETs for an ion hit in the channel center.

for comparison. As expected, the bipolar gain is higher for JL-SOI due to stronger FBE compared to IM-SOI. The bipolar gain decreases when the LET increases because the parasitic bipolar transistor enters in the high-injection regime. At very high LET, the bipolar
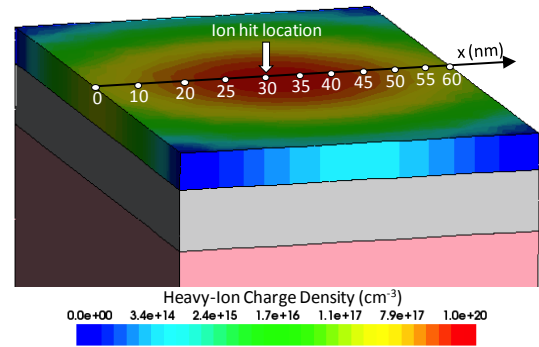

Fig. 5. 3-D profile of heavy-ion charge density in the silicon film of JL-SOI for an ion hit at x=30 nm and LET=1 MeV.cm^2/mg. Other positions for the ion strike considered in this work are also indicated. For a better view of the film, gate material, spacers and isolation oxide are not shown.
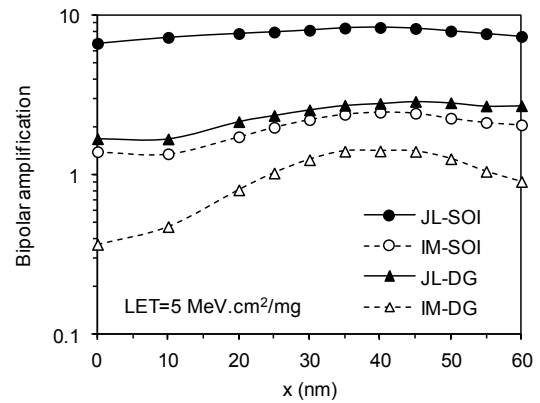

Fig. 6. Bipolar gain in JL-SOI, IM-SOI, JL-DG and IM-DG as a function of the ion hit location.

gain in JL-SOI decreases rapidly and becomes close to the values obtained in IM-SOI, JL-DG and IM-DG.

4.2. Dependence on the ion hit location

We also studied the dependence of the bipolar gain on the ion hit location along the channel (x axis). Several locations are considered between the source contact (x=0) and the drain contact (x=60 nm), as illustrated in Fig. 5. The 3-D profile of the heavy ion charge density in the silicon film is also shown in Fig. 5 for an ion hitting the film at x=30 nm (channel center). The current transient have been simulated for each x location and the collected charge was extracted from this transient. The bipolar gain is then obtained at a given LET for each x value. Figure 6 plots the bipolar gain dependence on the ion hit location for the four studied devices. The bipolar gain is always higher in JL-SOI than in IM-SOI, but has similar dependences on the ion hit location for all devices.

5. SEU in 6T SRAM cells: critical charge, threshold LET and scaling trends

For the four technologies, the 6 transistors of the SRAM cell (inset in Fig. 7) were entirely simulated in the 3-D device domain with the Synopsis/DESSIS module and were connected via the Mixed-Mode module [9]. Before simulating the SRAM cell we have determined for each technology the worst-case condition in terms of x location (along the channel) of the ion hit in the OFF-state NMOS. The worst-case location is the x location for which the collected charge is the highest. The worst-case x locations were found to be x=40 nm for both JL-SOI and IM-SOI devices. In the following, we used these worst-case locations for all SRAM cell simulations.

The time variations of the voltages extracted at nodes 1 and 2 (V_1 and V_2) for LET=3 $MeV.cm^2/mg$ are shown in Fig. 7 for JL-SOI and IM-SOI SRAM cells. For this LET value, the JL-SOI SRAM cell has flipped, while the IM-SOI SRAM cell did not flip.This result gives a first indication on the radiation hardness of JL-SOI technology: the SEU threshold LET of JL-SOI SRAM cell will be lower than that of IM-SOI, which means that the JL-SOI is more sensitive to radiation than the IM-SOI technology.

The SEU threshold LET (LET_{th}) of each cell was obtained by varying the ion strike LET until the SRAM cell was observed to upset. As expected, the critical charge Q_{crit}=0.126 fC and LET_{th}=1.35 $MeV.cm^2/mg$ are lower for the JL-SOI SRAM than for IM-SOI SRAM cell (Q_{crit}=0.205 fC and LET_{th}=3.15 $MeV.cm^2/mg$, [7]). In order to explain these results, we remind that Q_{crit} increases with the equivalent capacitance of the struck node (C_N), with the supply voltage (V_{DD}) and with the maximum current of the on-state PMOS transistor (I_{PMOS}), as explained in [10,11]. In our study, all cells are operating at the same V_{DD}. C_N is the same for JL-SOI and IM-SOI SRAM cells, but I_{PMOS} is lower in JL-SOI than in IM-SOI; this then explains why Q_{crit} is lower in JL-SOI than in IM-SOI SRAM cell. Q_{crit} and LET_{th} of JL-SOI are also lower than those corresponding to JL-DG (Q_{crit}=0.309 fC and LET_{th}=3.64 $MeV.cm^2/mg$) and IM-DG (Q_{crit}=0.51 fC and LET_{th}=7.48 $MeV.cm^2/mg$) obtained in [7].

Finally, we investigated the dependence of LET_{th} on the channel length, the power supply and, for JL-SOI SRAM cells, the film doping level. LET_{th} obtained for two channel lengths are shown in Fig. 8. Additional results for different V_D values and doping levels and a detailed discussion will be included in the full paper.
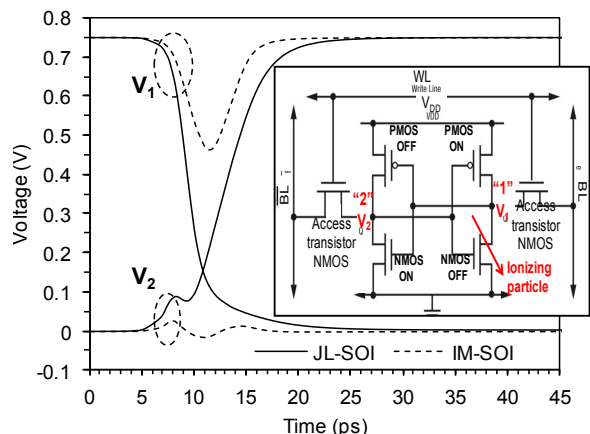

Fig. 7. Time variation of V_1 and V_2 in JL-SOI and IM-SOI SRAM cells at LET=3 $MeV.cm^2/mg$. Inset: 6T SRAM cell.
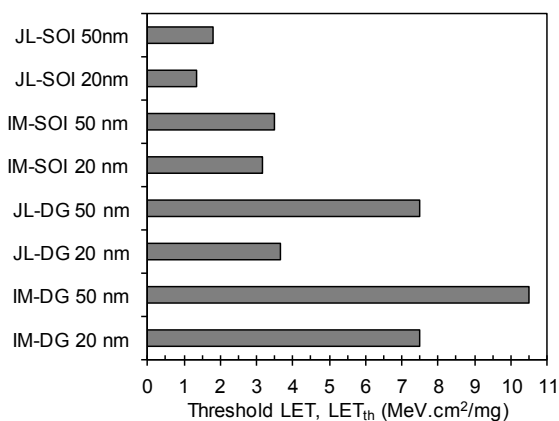

Fig. 8. Threshold LET of JL-SOI, IM-SOI, JL-DG and IM-DG SRAM cells for two channel lengths, L=20 and 50 nm.

References

[1]. R.C. Baumann, IEEE Trans. Device Mater. Reliab., vol. 5, no. 3, pp. 305-316, Sept. 2005.
[2]. S. Mitra, P. Sanda, and N. Seifert, IEEE VLSI Test Symposium, 2008.
[3]. C.-W. Lee et al. Applied Physics Letters 94 (2009) 053511.
[4]. J.P. Colinge et al. Nature Nanotechnology 5 (2010).
[5]. A. Kranti et al. Proc. ESSDERC, 2010, p. 357.
[6]. D. Munteanu and J.L. Autran. IEEE Trans. Nucl. Sci. 59 (2012) 773.
[7]. D. Munteanu and J.L. Autran. Microelectronics Reliability, vol. 54, pp. 2284-2288, 2014.
[8]. M. Vinet et al. IEEE Electron Dev. Lett. 26 (2005) 317.
[9]. Synopsys Sentaurus TCAD tools, Available online: http://www.synopsys.com/products/tcad/tcad.html.
[10]. P. Roche et al. IEEE Trans. Nucl. Sci. 46 (1999) 1354.
[11]. S.M. Jahinuzzaman et al. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 17 (2009) 1187.