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ORIGINAL PAPER

Optimization of Phosphorus Emitter Formation from POCl₃ Diffusion for p-Type Silicon Solar Cells Processing

H. Ghembaza[1] · A. Zerga[1] · R. Saïm[2] · M. Pasquinelli[3]

Abstract The main purpose of this work is to demonstrate the possibility of diffusion process perfection during silicon solar cells manufacturing by CFD simulation. Presently, the major community of PV industries uses a p-type silicon solar cell as the starting material. In this work too, boron doped silicon wafers are considered to form solar cells. Likewise, phosphorus oxy-chloride (POCl₃) is used as a precursor for phosphorus diffusion. To do this, we evaluate the throughput of an industrial low-pressure diffusion tube furnace in order to realize uniform emitters. The low-pressure tube furnace is designed to obtain emitter standard sheet resistances of about 60 Ω/sq and wafer uniformity less than 3 %. An up-to-date control model using for the first time a CFD numerical code has been derived from some previous work, to achieve better wafer to wafer temperature distribution. Moreover, a numerical process was built using an Atlas-Silvaco® TCAD Simulation Package where we can demonstrate that the short circuit current density (I_{sc}) increases from 4.97 to 6.53 mA/cm² compared to the conventional photovoltaic process. This (I_{sc}) enhancement can be attributed to the strong temperature effect on furnace atmosphere. Our result proves that we can target electrical properties of an emitter only by the manipulation and optimization of the doping profile. This process refinement is expected to contribute in the development of high efficiency conventional crystalline silicon solar cells considered for mass production.

1 Introduction

For the past few years silicon and silicon solar cells have been a focus point of worldwide researchers [1–7]. A compromise between cost reduction and efficiency improvement must be reached by using all semiconductor technology opportunities. This aim gives to the PV industry a better significance and competitiveness [8–14].

In general practice, solar cell emitters are obtained by phosphorus diffusion in p-type silicon inside a diffusion tube furnace under special conditions of temperature, pressure and gas flow thoroughly controlled in order to form an emitter able to ensure a good passivation of defects and at the same time to give to the contacts formed by serigraphy their ohmic aspects. Relations between emitter quality and electrical properties of crystalline silicon solar cells are considered strongly dependent [8–11].

For a long time, the PV industry have used a quartz diffusion tube furnace during the emitter formation process by the POCl₃ source in solar cells manufacturing. This is because one of the most important properties of quartz is its extremely low coefficient of expansion: 5.5×10^{-7} mm/°C (20–320 °C). This makes the material particularly useful for critical applications which require minimum sensitivity to

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Fig. 1 Schematic description of a usual diffusion tube furnace
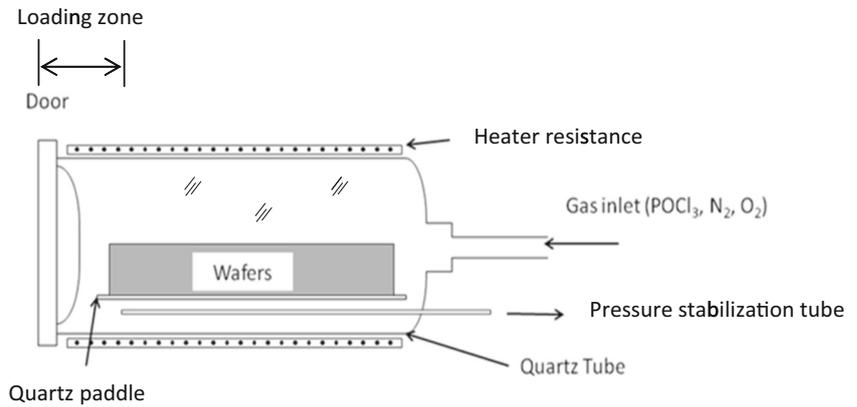
thermal changes. Also, we expect the process to be cleaner in a POCl$_3$ furnace because of the use of quartz boats [15].

Sadly, some problems of dopant homogeneity appear on the wafers surface consequently affecting the formed junction; a simulation of this furnace is thus necessary to optimize the thermal diffusion process in order to increase the quality of the formed emitter and thus to obtain an efficiency improvement of solar cells.

On the other hand, solar cell efficiency is drastically affected by Auger recombination in the emitter region. Experimentally, a high dopant concentration makes a layer named the 'dead layer' at the surface where the recombination velocities are very high. In this zone, there is an excess of non-electrically active phosphorous, which largely contributes to high emitter saturation current density and results in poor quantum efficiency in the short wavelength region [8].

2 Experimental Technique

2.1 Emitter Formation

The equipment of interest in this paper is a cylindrical diffusion tube furnace, shown in Fig. 1. In a quick description, the furnace contains along the circumference-wall several heating resistances separated in three zones. Each zone has an independent power source used to control the temperature of the batch. This is mainly because one of the most important parameters that controls the diffusion profile of phosphorus into the silicon matrix is the temperature.

This strong effect can be explained by the mathematical relationship between temperature and the coefficient of diffusion. This demands extreme care in maintaining a uniform temperature profile inside the diffusion furnace for consistent results. However, some authors observed that such furnaces have an inherent character such that their temperature profiles show a turbulent character at the loading zone of the furnace that could seriously affect the diffusion profile during the process [15].

The phosphorus diffusion process is carried out under a low-pressure atmosphere of about 0.3 bars. The wafers are vertically placed into a quartz support for loading 156 × 156 mm^2 square wafers. Every wafer is placed at a distance of about 3 mm next to each other. The support is placed into the quartz tube and is heated up to 810 °C. A flow of nitrogen is used as carrier for the liquid dopant source POCl$_3$ via a bubble trap. Before POCl$_3$ injection, O$_2$ gas is introduced into the diffusion tube to ensure the thermal oxidation of silicon. At high temperatures, phosphorus diffuses into the silicon matrix forming the p-n junction with the p-type substrate doped initially at 10^{16} cm^{-3} (0.1 Ω.cm of resistivity). All the wafers have a thickness of 200 μm.
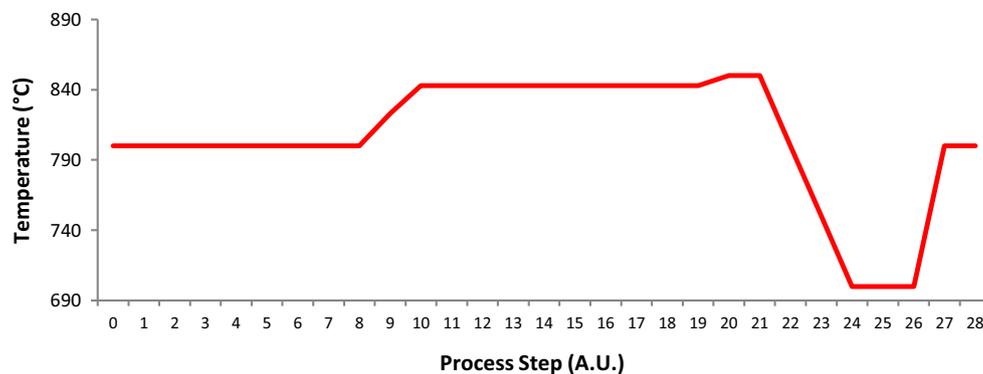
Fig. 2 Schematic single plateau temperature profile used in emitter formation
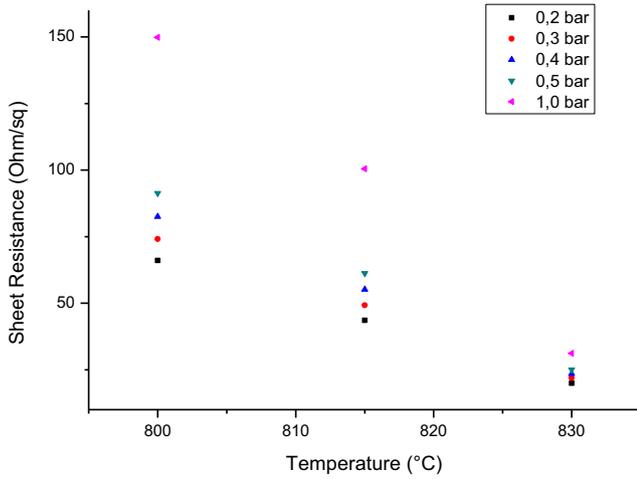
Fig. 3 Variation of sheet resistance versus temperature under different tube pressure. (A compromise between temperature and sheet resistance must be reached)

Usually POCl$_3$ diffusion standard recipes follow a temperature rise in a single-ramp from the stand-by furnace state to the pre-deposition temperature, then a second ramp to the drive-in temperature. Figure 2 is a schematic representation of the rise of the temperature profile currently used in the industrial photovoltaic process [16, 17].

To explain the relationship between emitter sheet resistance and the distribution of temperature at different pressures, we have conducted a simulation with a Silvaco® simulator [18] in accordance with conditions previously described.

Figure 3 includes the effect of pressure and temperature on emitter sheet resistance which is very important to understand the electrical properties of the emitter. The temperature range between 815 °C and 830 °C is the favorable working range with an acceptable sheet resistance for the photovoltaic industry. It may be noted that at 815 °C, POCl$_3$ diffusion at an atmospheric pressure leads to a sheet resistance of about 100 Ω/sq, which promotes the creation of active phosphorus precipitates and therefore an increase in dead layer thicknesses.

2.2 Modeling

In this paper, we consider the modeling and optimization of wafer temperatures by two ways: in a first stage, Computational Fluid Dynamics (CFD) models are used as a strong tool to investigate heat transfer and fluid motion inside the tube furnace. And in a second step, a TCAD simulation structure was built with an Atlas Silvaco® simulator to investigate electrical properties of solar cells.

In general practice, the CFD modeling process requires the following steps:

– Presentation of the mathematical equations describing the problem;
– Discretization and simplification of equations to produce numerical equations and define the application interval;
– Mesh generation by dividing the domain in small elements;
– Defining the initial and boundary conditions of the specific problem;
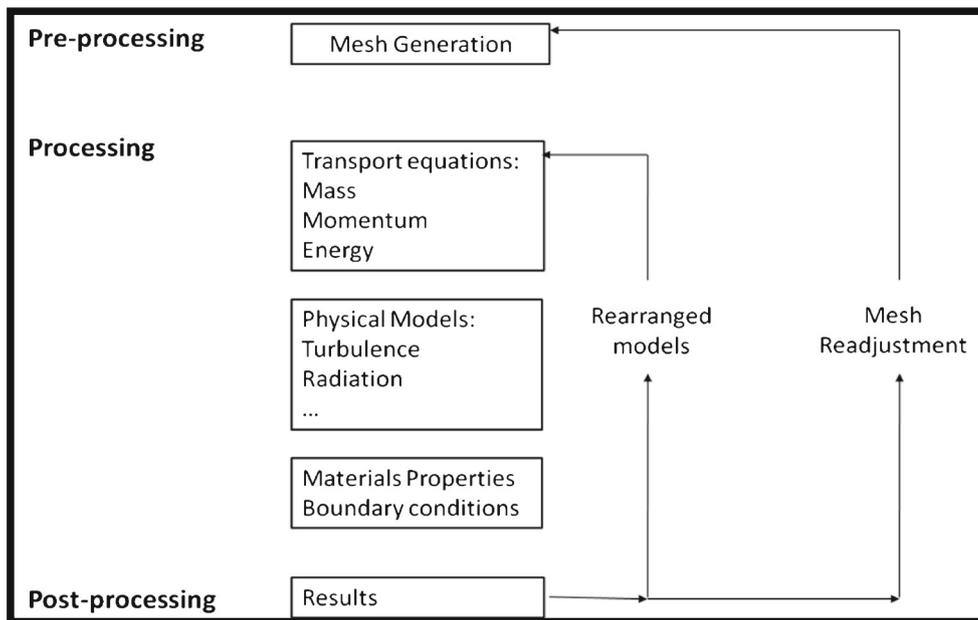
Fig. 4 Schematic CFD Modelling flow-charts

Fig. 5 Quartz tube furnace grid
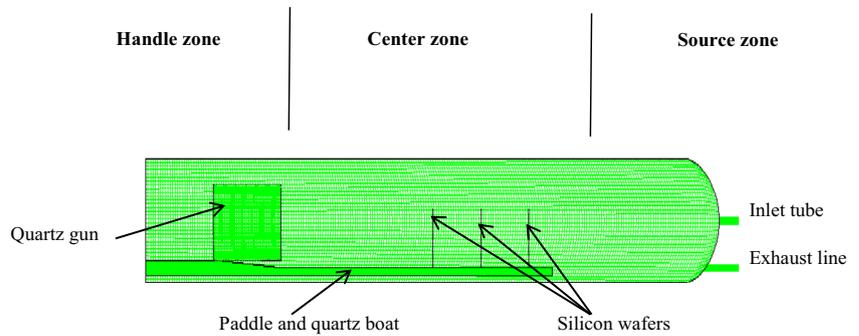
- Iterative problem solution is then obtained by convergence, stability and exact control of the proposed model.

Next, we built our flowchart according to the diagram shown in Fig. 4 by considering that all CFD codes contain the following three elements [19]:

1. A pre-processor, used to input the problem geometry and to generate the grid;
2. A flow solver, which is used to solve the governing equations of the flow subject to the conditions provided;
3. And a post-processor, which is used to show the results.

Figure 4 shows the CFD modeling flow-charts considered in our simulation.

2.3 Process Calibration

2.3.1 Mesh Generation

In order to simplify the problem, we consider a quartz tube with three positions for the wafers: at the 'source zone' near the inlet and exhaust tube, at the 'center zone' and at the 'handle zone' where the loading operation is run.

Figure 5 show the furnace structure after preliminary mesh generation. Note the three zones considered for electrical resistance heating: source, center and handle.

We start our simulation by building the mesh of our structure using the Gambit™ mesh generator [20]. A grid with about 685488 hexahedral cells and 1380570 nodes was created. The density of nodes is increased in the structure for a better computation of the thermal field.

Due to the high number of nodes and computational limitations, a laminar regime is considered for the transient simulation. The heat transfer by conduction, convection and radiation is calculated by using the Fluent™ Code. The radiative heat transfer is modeled by considering the "surface to surface" approach which is based on the calculation of radiation emitted from one zone to any other.

The vertical arrangement of silicon wafers causes radial temperature profiles during the heating and cooling process, this arrangement provides a thermal stress that could lead to plastic deformation of solar cells. The maximum heating rate desired is determined by the maximum thermal stress permitted for the specified wafer spacing. Using this same criterion the maximum cooling rate desired will generally not be attainable. The maximum cooling rate possible will be determined by the cooling rate of the complete furnace [21].

Fig. 6 Average tube furnace temperature versus position
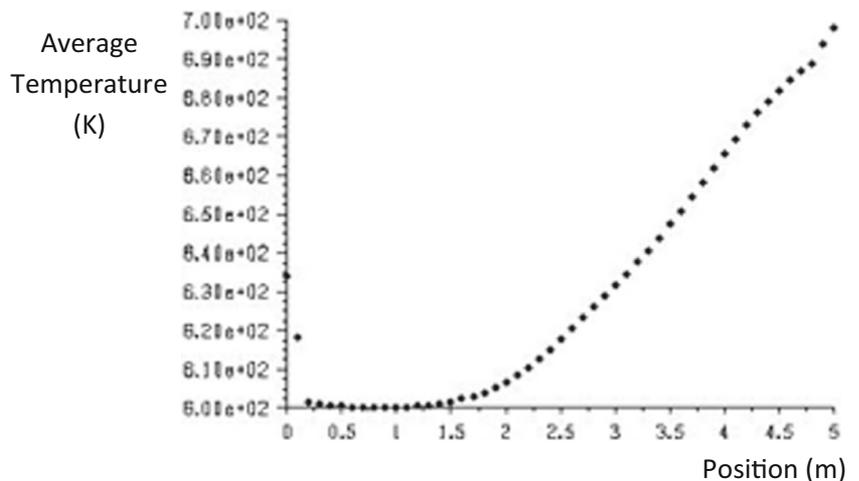
Fig. 7 Velocity vectors at the center zone [m/s], (time=2.5000e-01s)

Velocity (m/s)
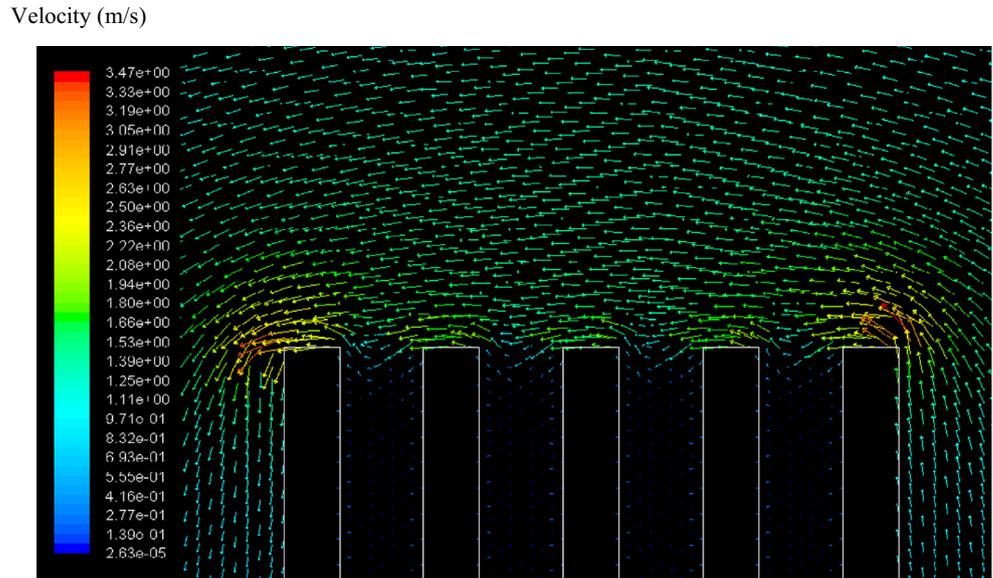
2.3.2 Transport Equation

Before we start our CFD simulation, a set of equations must be solved:

– The mass balance equation,
– The momentum balance or Navier-Stokes equation,
– The energy balance equation.

The energy equation and radiation heat exchange equation are solved for the three dimensional geometry of the diffusion tube by using the volume finite element method. The solution procedure uses the Simple (Semi-Implicit Pressure Linked Equations) algorithm which is one of the most common algorithms for incompressible flow calculations. This method is based on first guessing and then correcting the flow variables in an iterative manner to obtain the solution [19–21].

The boundary conditions are imposed from the physical structure in such a way that the temperature is imposed by the heating of the tube wall. The velocity is zero at the furnace wall, a specified mass flux at the inlet and a fixed pressure at the outlet was considered. We take into account a fixed value for temperature at the furnace sides in the region where the heating elements are placed and no heat flux through the walls outside this area. This supposition gives us adiabatic wall boundary conditions. The furnace pressure introduced in the momentumequations gives us the velocity components. Some corrections are made in order to satisfy the continuity.

Fig. 8 Pressure contour (zoom on the wafer arrangement. Wafer spacing is: 2.5 mm)
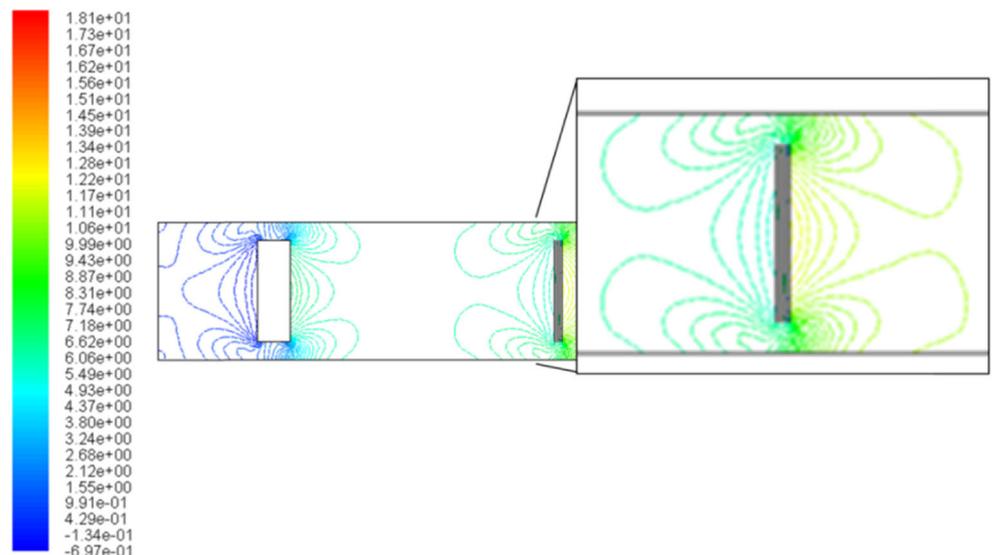
Fig. 9 The gas flow is directed near the inlet of the furnace [25]
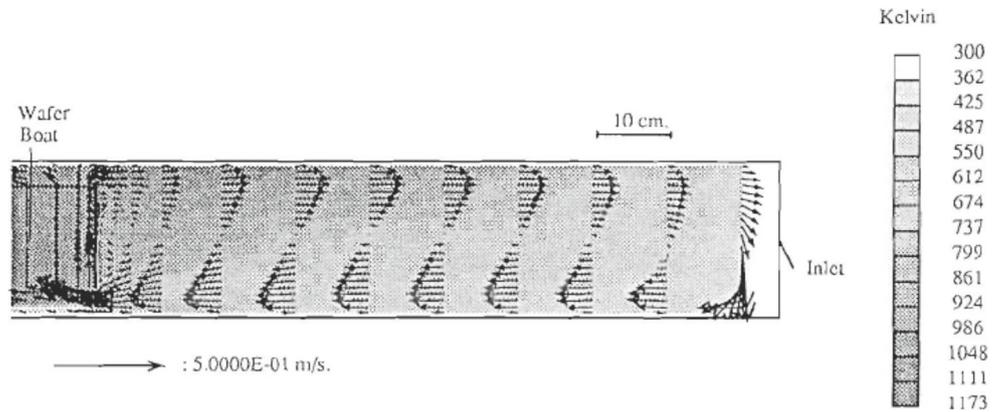
To describe the heat transfer to the wafer, we consider them in a first approximation as a block of porous matter. Next, we consider them to be a part of an infinitely long wafer load in an infinitely long tube. A complete description of heat transfer is achieved by constructing the energy balances for both the furnace and the wafers. It is postulated that this is an adequate description of the heat transfer inside the furnace [21]. There is clearly noted a large radial temperature gradient in the wafers block. However, we tried to keep this gradient as small as possible by adjusting wafer spacing and heating ratio appropriately.

3 Results and Discussion

3.1 CFD Modeling

We adjust our boundary conditions and we start our simulator code by taking into account our process calibration.

Considering these conditions, the convergence of the problem is established at the 63rd range of algorithm solution. Figure 6 shows the distribution of average temperature measured by thermocouples This temperature is significantly reduced at the 'source' zone. On the other hand, the general flow characteristics within the tube furnace are dominated by the circulating gas at the 'source' zone, this is the result of a large temperature gradient in this zone.

This result leads us to optimize the placement of heating sources and the solar cells emplacement since the axis of the furnace is subjected to lower temperatures than near the wall. The observed non-uniformity in temperature distribution is caused by the density difference between hot and cold gas flows.

The processing time and heating flow were kept constant; the carrier gas flow rate was varied from 1 l/h to 10 l/h. The simulator code allows us to get the contours of velocity near the solar cells wafer. Figure 7 shows the velocity contours in [m/s] near the wafers block. The colors are used

Fig. 10 Schematic multiple plateau temperature profile considered for TCAD simulation
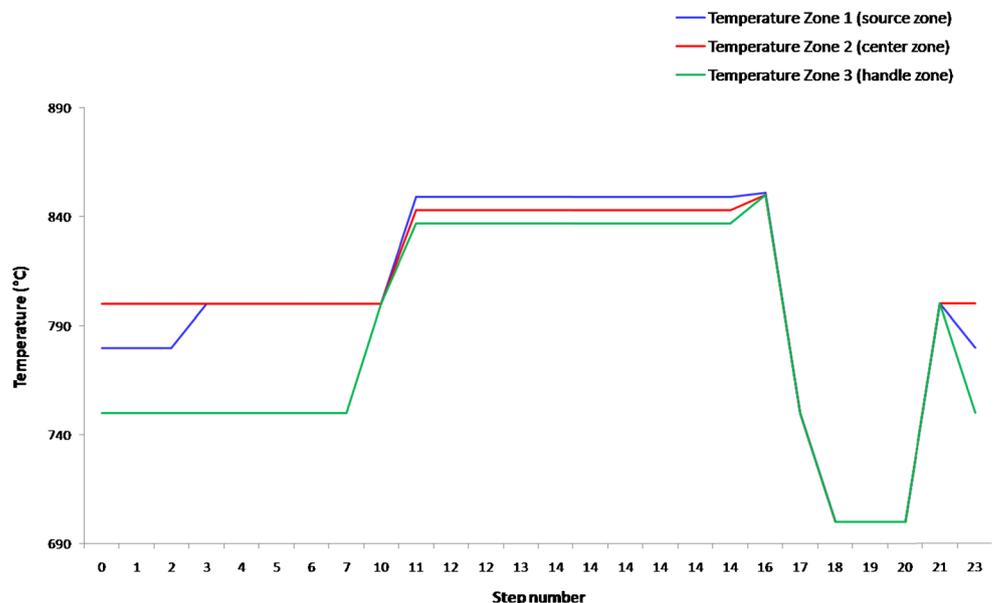
to indicate the increase in speed. It is easier to distinguish where the speed is high such as near the edges of the first and last silicon wafer. This result leads us to vary the wafers arrangement along the furnace for a better uniformity.

The surface doping concentration and junction depth of emitter are critical in order to provide the best yield. Panek et al. [22] obtained an emitter with 49 ohm/sq at a fixed carrier gas flow of 8 l/h, for the best output performance of a solar cell. The temperature range 830–860 °C is the ideal interval for an acceptable sheet resistance; this is confirmed by the values of the manufacturing industry [23].

Figure 8 represents the pressure contours at the center zone where the steady state is established. The insert shows a zoom of the wafers zone. The contour lines show clearly a pressure difference in the furnace near the solar cells block; this difference causes a recirculation of fluid flow and creates turbulence. A special characteristic of a low-pressure tube furnace is to improve gas flow motion and reduce the POCl$_3$ process time. This effect has been studied and confirmed by Goris et al. in [24].

This result is compared to the work of Howell et al. in [25], they demonstrate experimentally that near the inlet and the outlet zone, a recirculation of fluid flow is shown. Their results are shown in Fig. 9.

3.2 Temperature Distribution

In general practice, during semiconductor manufacturing a problem is encountered when we want to directly measure the wafer temperature. Estimates of these temperatures generated by the model based on thermocouple measurement are used in the control algorithm. So, an exact description of heat transfer in the furnace is a computational impossibility. Some authors give a number of postulates to simplify

this problem [25]. Because of the vertical arrangement of wafers, a radial temperature profile was created. This is mainly because the circumference heats much faster than the wafer's center.

For the CFD modeling, the heat transfer equation has been solved for different positions of wafers along the furnace batch, corresponding to several variations of the process step. The wafer spacing is varied from 1.5 to 3.5 mm. This arrangement gives to the wafer center a much better view of the heated wall. This is mainly because a cold mass flux can be introduced if the wafer spacing is larger. We can conclude that the wafer spacing/wafer diameters ratio influences the heating and cooling process. More than the loading zone is influenced by this parameter. Since as
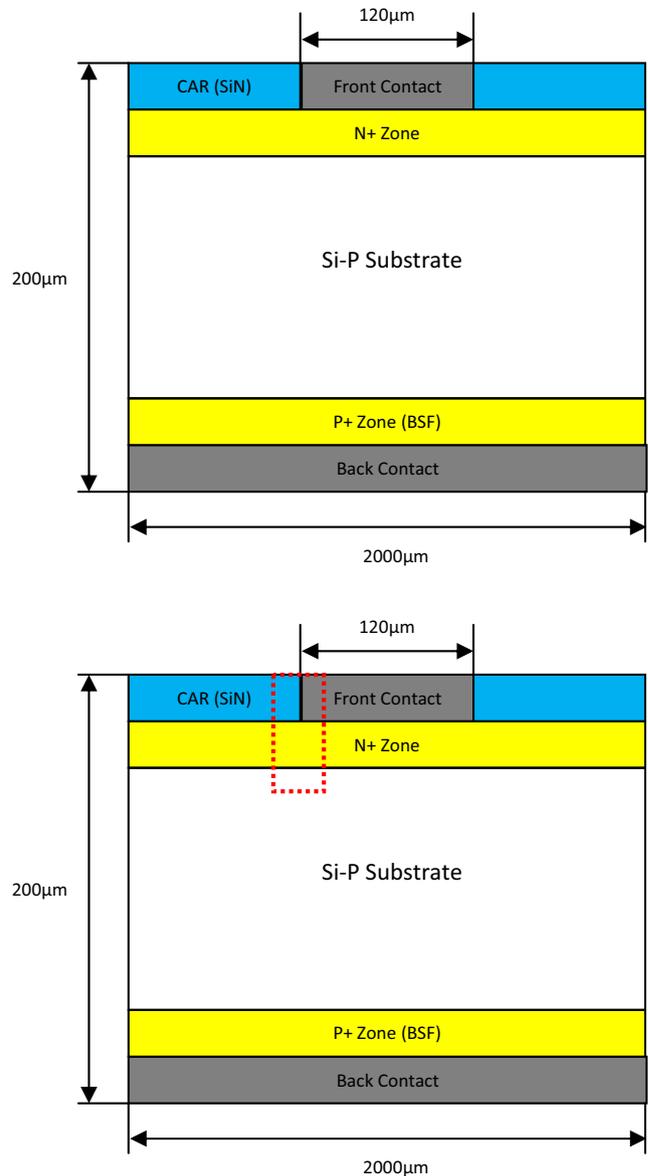

Fig. 11 Emitter sheet resistances v/s phosphorus concentration for POCl$_3$ diffusion

Fig. 12 Elementary solar cell structure. (The area with red dashed lines is the area' a')

the wafer first introduced has a few degrees of temperature more than the following one.

The same description of this phenomenon has been reported by Van Schravendijk et al. for an atmospheric furnace [21]. Franke in [26] reported a difference in temperature of 150 °C at the loading zone between the rim of the wafers and their centers.

From that result, we define a temperature recipe profile different from the conventional diagram currently used in the photovoltaic industry and represented by Fig. 2. These values were introduced in an Atlas Silvaco® program which allows us to evaluate the influence of temperature distribution on electrical characteristics of solar cells.

Figure 10 shows the temperature diagram considered for TCAD simulation presented further in Section 3.4.

3.3 Emitter Electrical Properties

The emitter is a zone where the Auger recombinations are maximal. Because Auger lifetime of carriers is inversely proportional to the square doping [27, 28] and becomes predominant for higher concentration of dopants the lifetime of minority carriers is significantly reduced [29, 30]. Since the emitter saturation current is also influenced by the recombination, these two factors, previously mentioned, have a direct relationship with the short circuit current density (I_{sc}) and open circuit voltage (V_{oc}) [31, 32].

To solve this problem the first resolution of researchers is to reduce the phosphorus doping concentration during emitter formation to limit losses by recombination. However, a low doping increases the resistive losses. The major tool for recombination evaluation in the emitter remains the

saturation current density. Consequently, special attention must be given to the evaluation of this parameter [8–10, 31].

We have evaluated the emitter sheet resistance as a function of the surface concentration at 825 °C for 1 hour as shown in Fig. 11. The sheet resistance decreases with increasing phosphorus concentration. This behavior is confirmed by some authors at 875 °C for 30 min [31, 32]. The relationship between sheet resistance and phosphorus concentration will be useful in our next simulation.

3.4 TCAD Modeling

To carry out the analysis of these parameters on the phosphorus profile and its influence on solar cell characteristics, we built a solar cell structure with the AtlasSilvaco® simulator at the same conditions of the process described in Section 2.1.

Figure 12 represents the elementary part of simulated solar cells and Fig. 13 represents a zoom on the emitter region (Area 'a') after TCAD simulation.

At every 'run' of the simulation program, we get the electrical properties of the solar cell and the (I–V) characteristic. By the combination of these results conducted for three temperatures corresponding to the three zones of the furnace (source, center and handle), as detailed in Fig. 10 we collect all the (Isc) for each simulated solar cell.

All the (I–V) characteristic are analyzed for every temperature ramp. The comparison of these parameters for the modeled solar cells under the Atlas Silvaco® simulation package leads us to an increase in the short circuit current (Isc). We obtained an enhancement from 4.97 to 6.53 mA/cm^2 compared to the conventional photovoltaic

Fig. 13 Modeled solar cell structure (zoom on area 'a' from Fig. 12)
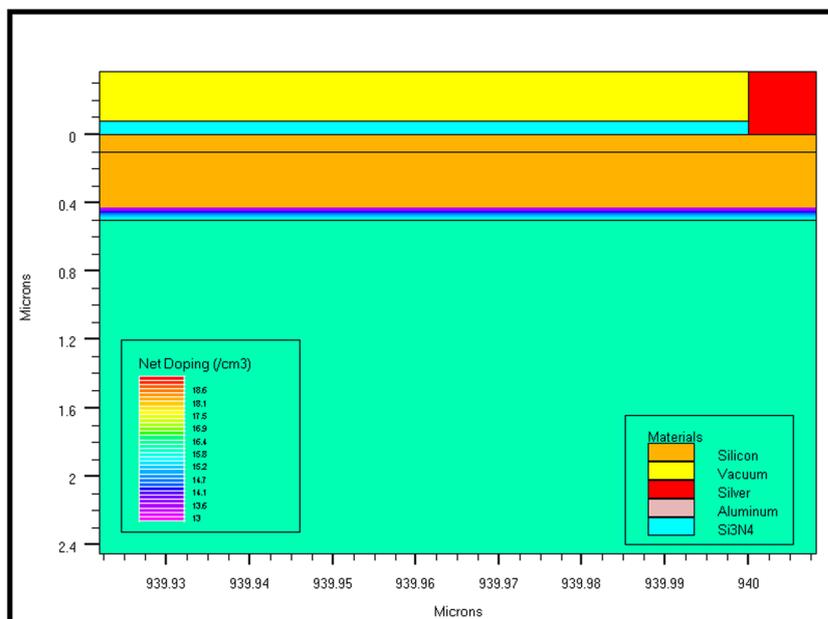
process with one ramp temperature. This (Isc) enhancement can be attributed to the strong temperature effect on the furnace atmosphere.

4 Conclusion

Nowadays, most industrial production lines apply a tube furnace diffusion using a liquid $POCl_3$ source for emitter formation. Optimization of this process involves a large number of parameters. Besides temperature and diffusion time, gas flux is an important one. An optimum heat transfer inside a quartz tube diffusion furnace during $POCl_3$ processing is difficult to obtain especially for a uniform temperature distribution if only experimental attempts are used.

In this paper, a numerical simulation of the diffusion process in a 3D steady-state modeling of heat transfer at low pressure is performed taking into account the main physical phenomena. Some geometrical and physical approximations of the real furnace and specific approaches for the thermal radiation modeling are used in order to solve the barriers and difficulties related to numerical simulation.

We start this study first by a CFD modeling of the tube furnace by providing a control model derived from some previous work and update to achieve more temperature distribution along the tube. TCAD modeling is next necessary to control monitoring of the diffusion process and solar cells electrical characteristics.

The CFD results show that an irregular temperature distribution is noticed especially at the loading zone of the furnace. Next, an optimized process is described using the Silvaco® TCAD simulation package by introducing the first CFD result. Although the optimization is still in progress, a promising increase in the (Isc) value from 4.94 to 6.53 mA/cm^2 has been reached compared to the conventional photovoltaic process.

Our result proves that we can target some electrical properties of crystalline silicon solar cells by a better CFD simulation of the so-called $POCl_3$ diffusion tube furnace. Controlling the formation of emitters by the variation of the diffusion parameters is therefore an effective way to improve the quality of emitters and an opportunity to increase the performance of mc-Si conventional solar cells.

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