New Strategies for Engineering Tensile Strained Si Layers for Novel n-Type MOSFET

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Abstract

We report a novel approach for engineering tensely strained Si layers on a relaxed Silicon Germanium On Insulator (SGOI) film using a combination of condensation, annealing and epitaxy in selected conditions well chosen based on elastic simulations. The study evidences the remarkable role of SiO_2 buried oxide layer (BOX) on the elastic behavior of the system. We show that tensely strained Si can be engineered by using alternatively rigidity (at low temperature) and viscoelasticity (at high temperature) of the SiO_2 substrate. In these conditions, we get a Si strained layer perfectly flat and free of defects on top of relaxed $Si_{1-x}Ge_x$. We found very specific annealing conditions to relax SGOI while keeping an homogeneous Ge concentration and an excellent thickness uniformity resulting from the viscoelasticity of SiO_2 at this temperature, which would allow layer by layer matter redistribution. Remarkably, Si layer epitaxially grown on relaxed SGOI remains fully strained with -0.85 % tensile strain. The absence of strain sharing (between $Si_{1-x}Ge_x$ and Si) is explained by the rigidity of the $Si_{1-x}Ge_x$/BOX interface at low temperature. Elastic simulations of the real system show that, due to the very specific elastic characteristics of SiO_2, there are unique experimental conditions that both relax $Si_{1-x}Ge_x$ and keep Si strained. Various epitaxial processes could be revisited in the light of these new results. The generic and simple process implemented here meets all the requirements of the microelectronics industry and should be rapidly integrated in the fabrication lines of large multifinger 2.5 V n-type MOSFET on SOI used for RF-switches applications and for many other applications.

Keywords: strained silicon, epitaxy, relaxation, condensation, MOSFET, carrier mobility,

1. Introduction

Strain engineering has long been an active area of development to enhance the key characteristics of Si MOS devices. There have been generally two different approaches. The first is a global or wafer scale pursued by IBM and then at Bell Labs to create a $Si_{1-x}Ge_x$ template from which a strained layer could be formed. As a consequence of the lattice misfit, defect management and complexity were difficult challenges to overcome. Industrialization was not realized. On the other hand, alternative approaches for planar MOS architectures included a tensile strained contact etch stop layer for NMOS. For PMOS, the substitution of Si with strained $Si_{1-x}Ge_x$ alloys within the source/drain regions has been widely adopted. Within the era of digital scaling, the minimum devices are extensively used to construct the basic building blocks of digital design. The aforementioned approaches are most effective with minimum geometries. Challenging notwithstanding, the wafer scale engineering retains the advantage that the benefit of the mobility enhancement can also be realized also with longer channel lengths (>150 nm). In one particular application of interest and the motivation for this study, RF switches constructed of cascaded NMOS in RF-SOI technologies could benefit from a reduction of the on-state resistance without significant compromise of power handling. The commonly used figure of merit for RF Switches is Ron × Coff (fs). Ron (Ω) is an indicator of the insertion loss of the RF signal between the antenna and the desired port and Coff (fF) is an indicator of the isolation between antenna and undesired ports. Both have to be as low as possible. The Ron is mainly limited by the channel resistance, thus one way to reduce it is to decrease the Gate length, but this approach is limited because the device has to sustain high power especially in OFF-state. The process developed in this study aims at highly improving the mobility whatever the channel length, and thus decreasing the Ron accordingly.

Tensile strained silicon has been proposed for more than twenty years as a booster of silicon-based CMOS transistors to improve the performance of very large scale integrated (VLSI) circuits independent of device geometry and scaling. It has been experimentally demonstrated that the effective electron mobility in MOS structures can be significantly enhanced using tensile strained-Si channel grown on $Si_{1-x}Ge_x$ relaxed buffer layer with an increase of Ion/Ioff ratio and more than 50 % transconductance enhancement in short-channel n-MOSFETs [1]; [2]; [3]; [4]; [5]; [6]; [7]; [8]. n-channel with mobility 75 % higher than in coprocessed bulk Si devices were reported, demonstrating that the mobility enhancement in strained-Si inversion layers was independent of vertical electric field. Furthermore, it was shown that the enhancement in carrier mobility observed at low lateral field did translate into improved performance at high lateral field [9]. In parallel, various theoretical calculations

also predicted an enhancement of the drive current and then of the speed [10] [11] [12]. The strain of the Si layer was shown to cause an increase in the electron mobility (up to factors of 1.5 and 1.9 for x = 10 % and 20 % respectively), over the entire range of transverse electric field $(E_{\perp})$.

Among the first works dedicated to strained silicon, [13] aimed at the fabrication of two-dimensional electron gas (2DGs) consisting of a strained Si well sandwiched between two $Si_{1-x}Ge_x$ relaxed layers and taking advantage of the 4.2 % misfit between Si and Ge crystalline lattice. Higher electron mobility was assumed to originate from changes in the band structure with carrier confinement in the Si layer. The biaxial tensile strain introduces splitting of degenerate bands, which results in smaller in-plane conduction mass and reduced intervalley scattering thereby yielding improved carrier velocity [14]. While an optimization of the structures could be achieved with an increase of the space thickness and lowering the carrier concentration and the background impurities, the main bottlenecks to be raised concern the large density of threading dislocations throughout the whole structure.

Most of the work carried out in the 2000s has been completed on $Si_{1-x}Ge_x$ relaxed substrate, trying to decrease the density of dislocations in the buffer and optimizing the associated surface roughness [15]; [16]; [17]; [18]; [19]; [20]. When the low-defect density $Si_{1-x}Ge_x$ relaxed buffers have been integrated into FETs, they have demonstrated high electron mobility in strained-Si and high hole mobility in strained-Ge (and Ge-rich alloys). *n*-MOSFET which have a simple epitaxial structure and require low Ge concentrations in $Si_{1-x}Ge_x$ relaxed buffer layers, represent the devices for which improvements of performances in short-channel devices are most important and best documented, with robust mobility and significant transconductance enhancements demonstrated on large scales [21]. The incorporation of a $Si_{1-x}Ge_x$ layer with a high Ge content was also shown to minimize the overall strain within the device and to produce optimized strained-Si/$Si_{1-x}Ge_x$ channel with even higher electrical performance in terms of transconductance, field-effect mobility and on-state drain current enhanced by up to 170 % while excellent off-state leakage currents and subthreshold characteristics [22]; [23]. This result was obtained without Chemical-Mechanical Polishing (CMP) step of the surface, while it is well-known that such process step is critical for transistor properties reliability [21].

Despite all the promising results obtained in research groups, so far, no technology based on strained-silicon could be transferred to production due to the unreliability of the process induced by the formation of misfit dislocations during the various subsequent steps of the process. In fact, published drive current I_{on} enhancements are at most 15 % – 20 % for $L_{gate} \approx 100$ nm. Then more attention should be devoted to the optimization of several parameters besides mobility and CMOS process for strained-

Si. So far, the various approaches under progress produce considerable variations in device performances. While the quality of the strained-Si epitaxial layer is usually directly linked to the underlying $Si_{1-x}Ge_x$ relaxed buffer layer (threading and misfit dislocations density and surface morphology), in manufacturing, many other criteria have to be checked, for example uniformity of Ge-content and Si thickness to ensure consistent transistor performances on large scale wafers. But also, the level of Ge content in the $Si_{1-x}Ge_x$ virtual substrate which is decisive for the electron mobility of *n*-MOSFET, since it sets the amount of strain-induced splitting between the Δ2 and Δ4 valleys in the Si layer.

It is therefore essential to study in detail the influence of the different conceptual parameters of the system under consideration. As regards Ge content, in some studies it was reported that the mobility monotonically increases with strain up to $x \approx 0.2$ (strain 0.8 %) and then saturates. This is because at this strain level, the conduction-band splitting is sufficient to completely suppress intervalley phonon scattering, and thus only little enhancement of electron mobility could be gained at higher strain [24]. In other studies, an enhancement of the electron mobility by ≈ 120 % was measured for $x \approx 0.30$, despite the large misfit (between Si and $Si_{1-x}Ge_x$) causing high density dislocations. Monte Carlo simulations attributed these discrepancies to additional electron mobility-limiting mechanism such as defect scattering (surface roughness and high density of defects) in the epitaxial strained-Si/$Si_{1-x}Ge_x$ system [25]. Simulations results were confirmed by the comparison of mobilities measured on systems before and after CMP. It was shown that CMP eventually followed by epitaxy of thick silicon, significantly improves mobilities, when compared to devices without CMP [21]. The thickness of the strained Si layer has also a strong influence: under low effective field, as this thickness decreases, the number of electrons in the $Si_{1-x}Ge_x$ and close to the SiO_2/Si interface increases, creating parasitic conduction and scattering events that degrade the overall mobility. Under high effective fields, the electrons are all located in the strained Si layer and the Si thickness has no influence on the mobility. For NMOS devices the Si thickness should then be larger than ≈ 10 nm [26].

More recently, the combination of tensile strained silicon with $Si_{1-x}Ge_x$ on insulator (SGOI) has been proven to offer new opportunities to increase the devices performances. New efforts were made to transfer the advantages obtained in bulk CMOS technology to insulating substrate [27]; [28]; [29]; [30]; [31]; [32]; [33]. However, the measured values of ohmic mobilities that can be as high as 53105 $cm^2V^{-1}s^{-1}$ at low temperature, were shown to strongly depend on the interface roughness and on the material quality. In general, the mobility characteristics of n-MOSFETs fabricated on strained-Si layers

transferred to insulating handle wafers has been found to be nearly identical to those on $Si_{1-x}Ge_x$ graded buffers. The main reason for this is that generally, the fabrication process of the strained-Si/$Si_{1-x}Ge_x$ relaxed buffer layer remains the same, while only a transfer step of $Si_{1-x}Ge_x$ on SOI is added. Indeed, the tensile strained Si in the channel on BOX has been generally implemented following only two ways: 1) making strained Si/relaxed $Si_{1-x}Ge_x$ on buried oxides using layer exfoliation to transfer the relaxed $Si_{1-x}Ge_x$ buffer on SOI; 2) bonding and transfer the strained Si layer directly on the BOX. Another method using SIMOX process was suggested but it is limited to $x \leq 0.1$ which is then not useful for most of the microelectronic applications.

In this work based on elastic simulations we show that tensile strained Si can be engineered by alternatively using rigidity (at low temperature) and viscoelasticity (at high temperature) of the $Si_{1-x}Ge_x/SiO_2$ interface. We then demonstrate both theoretically and experimentally an original and simplified process that should be easily integrated in NMOS device for the fabrication of tensile strained Si layer. We show that using a combination of epitaxy and condensation steps in very specific experimental conditions (i.e. low temperature $Si_{1-x}Ge_x$ condensation and high temperature annealing) we can get strained Si layer perfectly flat and free of defects on top of relaxed $Si_{1-x}Ge_x$. In very specific annealing conditions $Si_{1-x}Ge_x$ layer (on BOX) is relaxed, while keeping an homogeneous Ge concentration ($x \approx 20$ %) and an excellent thickness uniformity. This results from the viscoelasticity of SiO_2 at this temperature, which could allow layer by layer matter redistribution. Cross-section High Resolution Transmission Electron Microscopy (HRTEM) images highlight the very flat surface/interface and the absence of extended defects. Another very interesting result is that the Si layer grown on top of this relaxed $Si_{1-x}Ge_x$ remains fully strained with - 0.85 % tensile strain measured in the layer, by both geometrical phase analyses (GPA) of HRTEM images and interatomic lattice plane distance measurements. The absence of strain sharing (between $Si_{1-x}Ge_x$ and Si) is explained by the rigidity of the $Si_{1-x}Ge_x$/BOX interface at low temperature (Si epitaxy at 500 °C). In more detail, the elastic nonlinear simulations of the real system in our experimental conditions show that for $Si_{1-x}Ge_x$ ($x = 0.2$, $e = 19$ nm) the maximum thickness up to which there is no relaxation of the Si top layer is 83 nm.

Due to very specific elastic characteristics of SiO_2, we have found unique experimental conditions that both relax $Si_{1-x}Ge_x$ and keep Si strained. The generic process implemented here can be easily integrated in the fabrication lines of large multifinger 2.5 V n-type MOSFET on SOI used for RF-switches

applications and meets all the requirements of the microelectronics industry for many other applications. The generic behavior found could be applied to many other heteroepitaxial systems.

2. Materials and methods

The process for the fabrication of tensile strained Si layer is schematically illustrated in Figure 1. The investigated SOI wafers are commercially available from SEH. The investigated structures were fabricated in state of the art 200 mm technology semiconductor facility of XFAB France. They initially consist of a 140 nm thick top-Si layer on top of 400 nm thick BOX (Figure 1a). The function of the poly-Si layer under the BOX is to suppress harmonic generation primarily from the active devices and to improve the linearity of RF switch devices. It is commonly referred to as a "trap-rich" layer. The 400 nm-thick BOX consolidates this effect and also provides isolation between back side and front side. The top Si layer is first locally thinned using LOCOS process followed by a wet etch to reach 20 nm. Thickness uniformity and surface flatness are systematically controlled over the entire wafer by ellipsometry. A thickness inhomogeneity lower than 8 % over the whole 8" wafer was found. At first, 20 nm $Si_{1-x}Ge_x$ film with x = 0.15 is epitaxially grown by Solid Source Molecular Beam Epitaxy (MBE) in a 200 mm UHV growth chamber (SG800 model from DCA Instruments) after ex situ chemical cleaning and in situ thermal cleaning (Figure 1b) that consist of chemical oxidation (2 to 8 min HF etching) and thermal annealing (at 500 °C for 10 min) steps respectively. Si and Ge fluxes are produced with solid sources using e-beam evaporator and effusion Knudsen cell for Si and Ge respectively. The growth rates are monitored in situ by RHEED. Si and Ge growth rates are 1 nm min^{-1} and 0.1 nm min^{-1} respectively. The growth temperature is set at 400 °C for both $Si_{1-x}Ge_x$ and Si.

Next, thermal oxidation in O_2 atmosphere is carried out in a Rapid Thermal Oxidation (RTO) furnace at low temperature (typically 750 °C). During this step the selective oxidation of only Si atoms, leads to the formation of SiO_2 on the top of the structure and to the repulsion of Ge atoms underneath the SiO_2, resulting in a pile-up of Ge at the $SiO_2/Si_{1-x}Ge_x$ interface (Figure 1c). Oxidation is carried out during 70 min to obtain a 10 nm thick $Si_{1-x}Ge_x$ layer with a Ge concentration about 50 %. The wafer is then furnace annealed (Rapid Thermal Annealing) under inert nitrogen atmosphere. RTA of these samples were done at various temperatures and N_2 pressures. This treatment promotes the interdiffusion between Si and $Si_{1-x}Ge_x$ and leads to the homogenization of Ge concentration across the $Si_{1-x}Ge_x$/Si heterostructure (Figure 1d). As a result, $Si_{1-x}Ge_x$ and Si layers mix to form a homogeneous $Si_{1-x}Ge_x$ layer with a lower fraction of Ge and a total thickness thinner than the initial ($Si_{1-x}Ge_x$ + Si)

one. Small thickness is a key parameter to favor strain relaxation by gliding and redistribution of matter at the interface (see discussion). In addition, since the total amount of Ge in the SGOI layer is preserved throughout the process, the final Ge concentration in SGOI can be easily estimated ahead of time. Condensation time is then fitted to obtain a final SGOI concentration of x ~ 0.25 that is enough to efficiently stress the silicon top layer. It also has a sufficiently low thickness (< 20 nm) to avoid nucleation of dislocation and facilitate elastic strain relaxation (see simulations part) during the annealing step.

The last crucial step is the re-epitaxy of silicon. This is done after chemical etching of SiO_2, i.e. by dipping the sample in a HF diluted solution (Figure 1e). A film of 70 nm Si is epitaxially grown in MBE at low temperature typically 500 °C (Figure 1f).

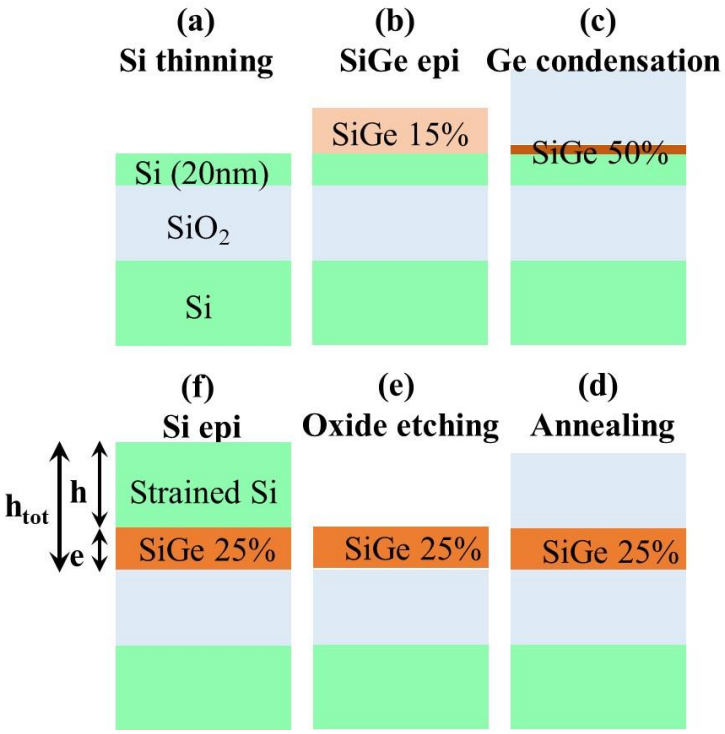


Figure 1: Process flow diagram: (a) Nominal substrate after Si thinning; (b) $Si_{1-x}Ge_x$ epitaxy; (c) Ge condensation during RTO; (d) Furnace annealing for homogenization (950 °C); (e) Chemical etching of oxide; (f) Si epitaxy

The industrial developments require accurate and reliable metrology methods for the characterization and subsequent control of the magnitude of strain (relaxation) in the s-Si layer ($Si_{1-x}Ge_x$ buffer) and the Ge content (x). To this end, Transmission Electron Microscopy (TEM), Energy Dispersive Spectroscopy (EDS) and Geometrical Phase Analysis (GPA) are the only analyses that give

simultaneously and locally these parameters. Thickness and crystal quality of the SGOI layer were assessed by cross-section TEM. TEM specimens were prepared by Focused Ion Beam (FIB) milling using a dual-beam FEI Helios 600 NanoLab. The strain distribution throughout the films is imaged and mapped using GPA. High Resolution-TEM observations were performed using a Microscope MET FEI Titan 80-300 with Cs corrector operating at 300 keV. Transmission Electron Microscopy (TEM), Scanning Transmission Electron Microscopy and High-Angle Annular Dark-Field imaging (STEM HAADF) and Energy-Dispersive X-ray Spectroscopy (EDS) were done using a FEI Tecnai G2. Most of the strain values are given relatively to the reference (unstrained Si lattice from the substrate under the BOX). When the BOX is too thick, the reference is taken in the $Si_{1-x}Ge_x$ layer whom Ge composition is estimated by EDS. More generally EDS using GATAN semi-quantitative analyses is used to estimate the Ge concentration throughout the films after the various fabrication stages.

3. Results and discussion

3.1 Strain determination

We start the process by the epitaxy of a $Si_{1-x}Ge_x$ film with a low Ge concentration (x = 0.15) to avoid the formation of dislocation during the various fabrication stages. Epitaxial $Si_{1-x}Ge_x$ layers with x ≥ 25 % could not be used because of the formation of dislocation during the process. Figure 2 gives a cross-section overview of the whole system including Si(001) substrate, poly-silicon, 400 nm thick BOX and $Si_{1-x}Ge_x$/Si top layers. The STEM HAADF (Figure 2a) highlights the dislocations and extended defects in thick polysilicon underneath the BOX. The quality of the epitaxy and the absence of defects can be assessed on Figure 2b which gives a magnified view of the Si/$Si_{1-x}Ge_x$ epitaxy.

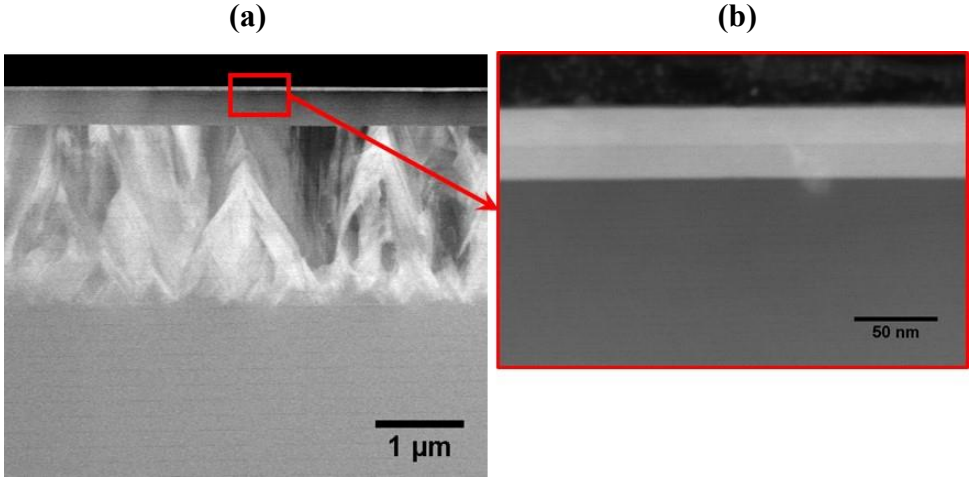


Figure 2: STEM HAADF cross-section images of: (a) the whole structure; (b) The Si/$Si_{1-x}Ge_x$ epitaxy.

The semi-quantitative analysis of the layer composition is made by EDS (Figure 3a). The elemental depth analyses profiles of Si, Ge and O highlight the uniformity of the Ge composition across the layer and the abruptness of the $Si_{1-x}Ge_x$/SOI interface resulting from the L.T. MBE growth process (T = 500 °C). The layers thickness and composition can also be deduced from the line profiles. Both the thickness (20 nm and 24 nm measured for Si and $Si_{1-x}Ge_x$ respectively) and the Ge concentration (x = 0.15) perfectly fit with the nominal parameters. The corresponding diagram summarizes the starting structure (Figure 3c).

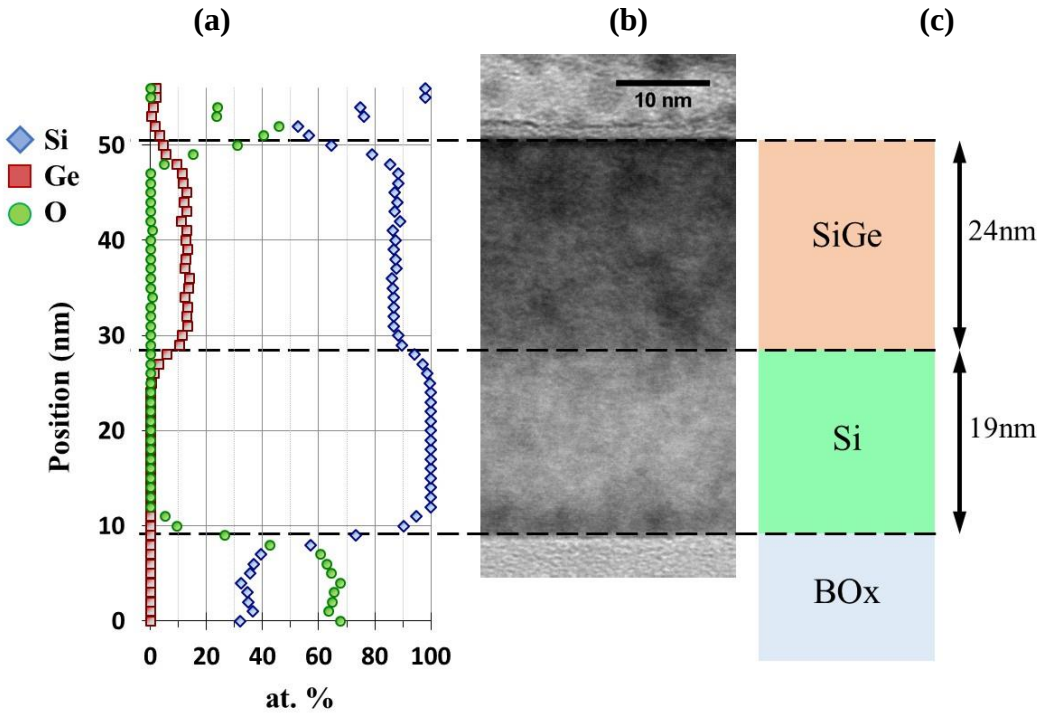


Figure 3: (a) EDS line profile of the elemental composition of the layers; (b) TEM diffraction contrast; (c) Diagram of the structure with the deduced thickness.

Condensation is commonly carried out during dry thermal oxidation at high temperature (H.T.) typically between 1000 °C and 1200 °C. However, during H.T. oxidation, dislocations nucleation is easily promoted [34]; [35]; [36] together with the buckling of $Si_{1-x}Ge_x$ layers due to the viscous flow of oxides surrounding the $Si_{1-x}Ge_x$ layers [37]. We reported recently, that fully strained and free of

dislocations Ge rich layers (GRL) with flat surface and abrupt interface, can be fabricated using low temperature condensation [38]; [39]. In these experimental conditions, the basic mechanism of GRL formation is a self-limited interdiffusion process regulated by the entropic term of the formation energy which is minimum at $Si_{0.5}Ge_{0.5}$ at the expense of the elasticity driven interdiffusion. The process developed provides an easy and efficient way to produce planar GRLs with remarkable elastic features. It also enables the total inhibition of the morphological instability (which commonly develops during the growth of $Si_{1-x}Ge_x$ on Si [40]; [41]), together with the hindering of dislocations for critical thickness much larger than the ones commonly obtained by direct deposition. Those behaviours were explained by the injection of self-interstitials in the GRL during condensation.

The present process takes advantage of this fabrication of GRLs, fashioning them for the fabrication of relaxed $Si_{1-x}Ge_x$ template layers with lower Ge concentration, best suited to the device targeted here. The first condensation tests were performed at 800 °C using a test sample constituted of 25 nm BOX and 19 nm $Si_{1-x}Ge_x$/SOI. The reduced thickness of the BOX allows for more reliable GPA strain measurements. A cross-section TEM image of the resulting structure is given in Figure 4 together with the EDS line profile. They both evidence the presence of an ultra-thin Si layer (4 nm) between the $Si_{1-x}Ge_x$ and the BOX layers, remaining from the SOI layer. From previous studies, we know that this ultra-thin layer has strong interactions with the BOX and maintains the top layer fully strained. Ge concentration is about 40 % (lower than the 50 % concentration obtained at temperatures < 800 °C) and has a diffuse interface with the Si layer as already observed in [38] [39]. There is no relaxation and no dislocations in the layers.

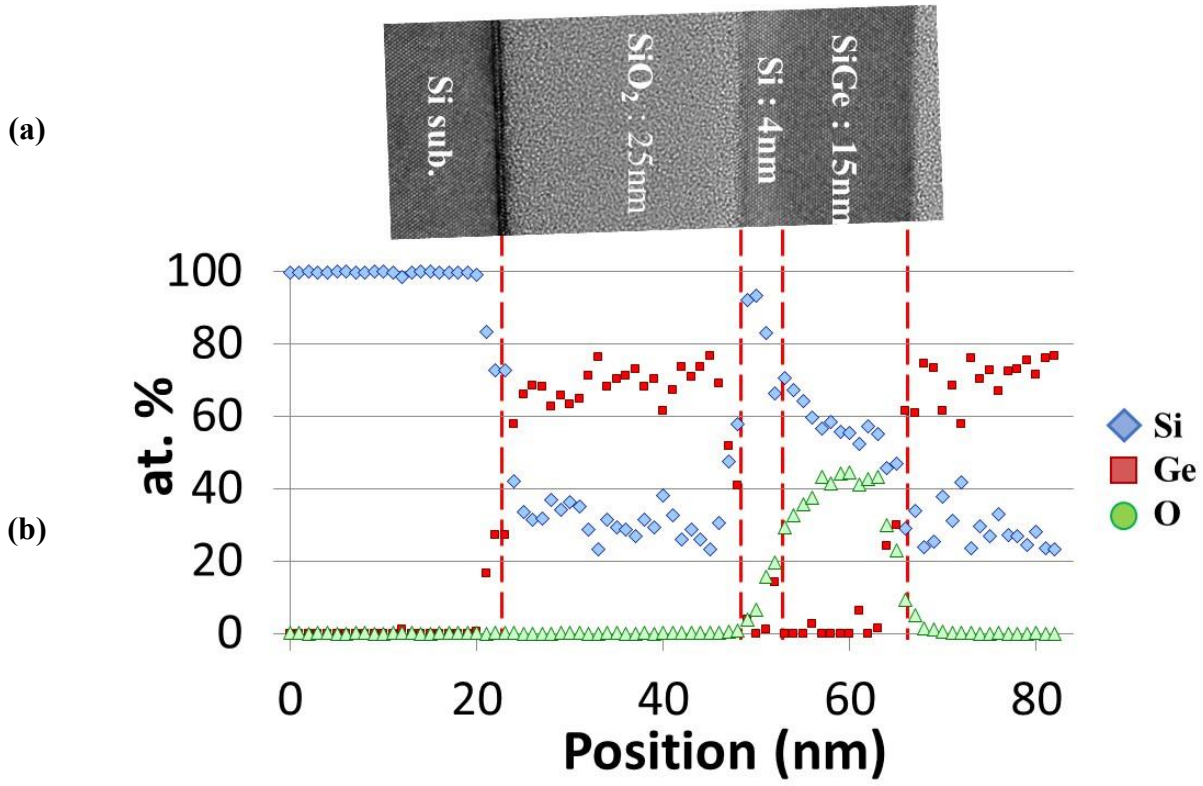


Figure 4: (a) TEM cross-section image of the structure after condensation at 800 °C; (b) Corresponding EDS line profile of Si, O and Ge.

For the next step, the best mixing/homogenization results are obtained for an annealing temperature of 950 °C in RTA under N_2. This method produces a strong intermixing and a homogeneous $Si_{1-x}Ge_x$ layer (Figure 5); it also promotes atomically flat interfaces (between the cap $SiO_2/Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x$/BOX) and low surface roughness. The $Si_{1-x}Ge_x$ RMS roughness measured on the AFM image over 10 × 10 μm^2 is below 0.1 nm (below the AFM resolution) indicating the efficiency of the method to produce high quality $Si_{1-x}Ge_x$ relaxed template layer. The plateau in the EDS line profile confirms the uniformity of the Ge composition across the film (Figure 5b). A Ge concentration of 23 % is extracted by EDS semi-quantitative analysis.

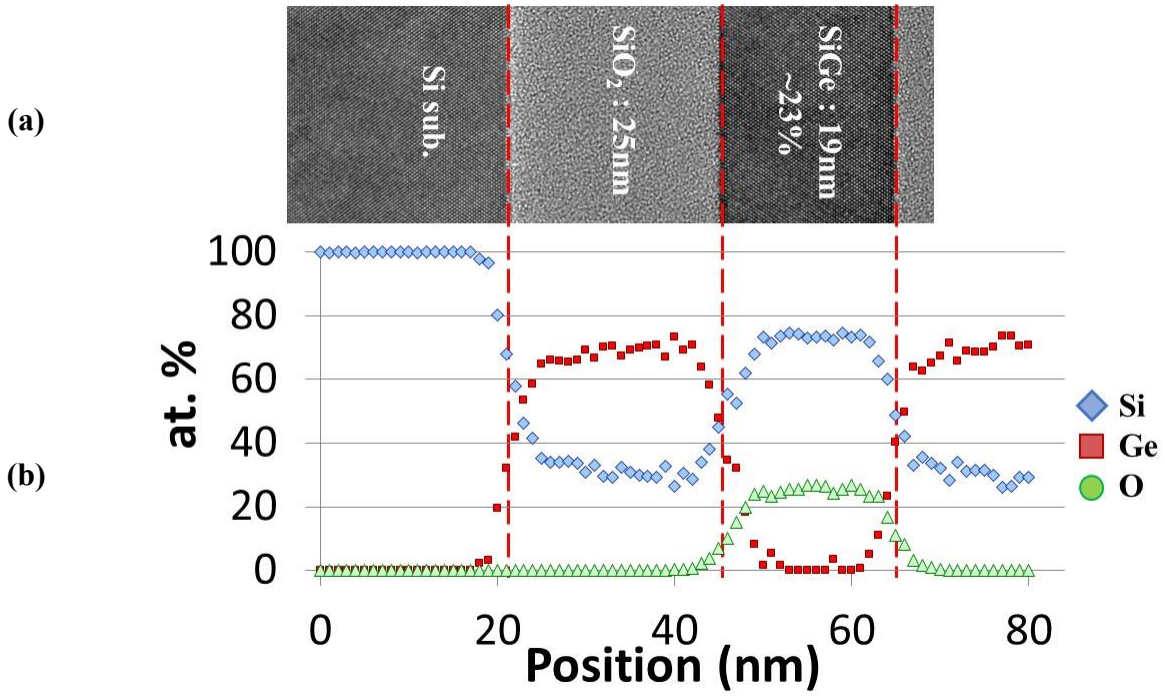


Figure 5: (a) TEM cross-section image of the system after homogenization; (b) Corresponding EDS line profile of Si, O, and Ge.

It should be noted that the annealing temperature was chosen to lie well below the solidus line of the Si-Ge alloy phase diagram, thereby avoiding the formation of dislocations. Higher temperature annealing, resulted in nucleation of dislocations, as already observed in previous studies [42]; [43]. Fabrication of structures with partially relaxed layer free of defect were achieved for $Si_{1-x}Ge_xOI$ with x = 0.15. For larger Ge concentrations, the layers were defective (formation of dislocations during annealing).

A critical step is the stress relaxation in the $Si_{1-x}Ge_x$ layer upon annealing. To quantitatively map the c-lattice (a-lattice) strain on both sides of the BOX, we use the High Resolution TEM image shown in Figure 5a. GPA is then performed to the image by applying the method described in [44]. We can note artefact values of strain close to the interface with the amorphous SiO_2. They are related to the integration of pixels including both crystalline and amorphous cells in the analysis. Figure 6a shows the resulting color-coded map of $\Delta c/c$ ($\Delta a/a$) in the $a-c$ directions. The left part corresponds to the unstrained Si substrate ($\Delta c/c = \Delta a/a = 0$ %). The right part features a deformation in the c-direction ε_{yy} = + 1.5 % and a-planes ε_{xx} = + 0.8 % with respect to Si (Figure 6b). These values correspond to partially relaxed $Si_{1-x}Ge_x$ x = 0.23 as found by EDS. Unlike the sample before annealing, the distribution of the mechanical strain is constant across the layer. Importantly, while a partial relaxation is already

obtained, there is no discontinuity (or defects) in the interfacial regions for $\Delta c/c$ and $\Delta a/a$, confirming the absence of misfit dislocations at the interface. This purely elastic relaxation is therefore the result of a sliding interface as already reported [36]. Overall, while GPA reveals a partial relaxation it also shows that 10 min annealing (950 °C) is not sufficient to achieve full relaxation (that would induce ε_{xx} = 1 % and ε_{yy} = 1 %) and not even the relaxation requested to significantly increase the electrons mobility.

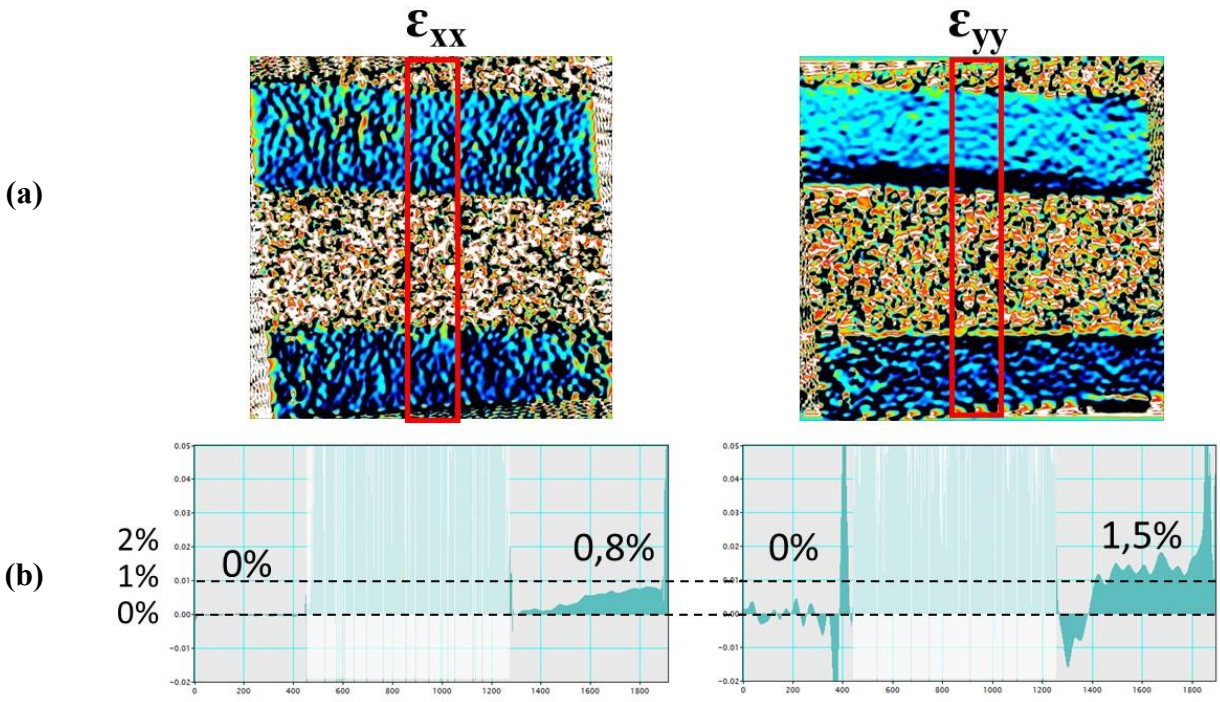


Figure 6: (a) Color scale map of *c*-planes (ε_{yy}) and *a*-planes (ε_{xx}); (b) Distribution of strain integrated on areas pointed by the red squares in (a).

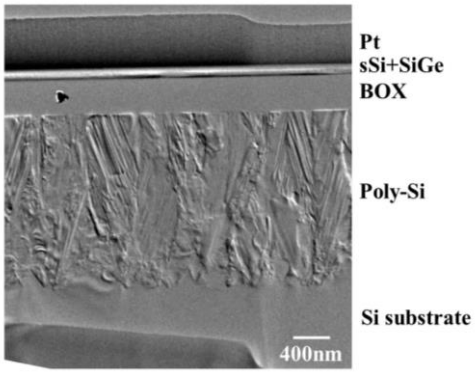
Several test samples were needed to validate the condensation/annealing method for forming a buffer as relaxed as possible (but without the nucleation of dislocations), the optimal annealing conditions found were: T = 970 °C, t = 30 min. The process generates an + 0.85 % relaxation of the $Si_{1-x}Ge_x$ and ensures the absence of nucleation of dislocations during the subsequent steps.

These conditions are used on the XFAB pilot samples on the bench tests. On these samples, quantitative GPA of strain is made difficult due to the excessive thickness of the oxide which makes impossible to use the Si substrate as a reference (as a matter of fact, HR images cannot include in the same image

both the top Si/$Si_{1-x}Ge_x$ layers and the substrate). We then used $Si_{1-x}Ge_x$ as a reference for GPA and the Ge concentration is deduced by EDS (x = 0.20 in these conditions).

A large-scale SEM image of the device where all the constituents of the system, including poly-silicon, BOX, $Si_{1-x}Ge_x$ + Si and Pt cap layer are visible, is given in Figure 7a. The HR-TEM image of the square area evidences the perfect crystalline quality of the sample on large scale (Figure 7b). Even more interestingly are the color-coded GPA maps of the Si/$Si_{1-x}Ge_x$ which evidence a constant strain from $Si_{1-x}Ge_x$ to Si in the direction parallel to the surface and an abrupt change between $Si_{1-x}Ge_x$ (set by calibration at ε_{yy} = + 0 %) to the tensile strained Si (Figure 7c). From this analysis (taking $Si_{1-x}Ge_x$ as reference) we find a tensile deformation of the Si layer $\varepsilon_{xx} = 0$ ($\Delta a/a$) and ε_{yy} = - 0.78 % ($\Delta c/c$), not so far from the expected fully relaxed value (ε_{yy} = - 1.1 %).

(a)



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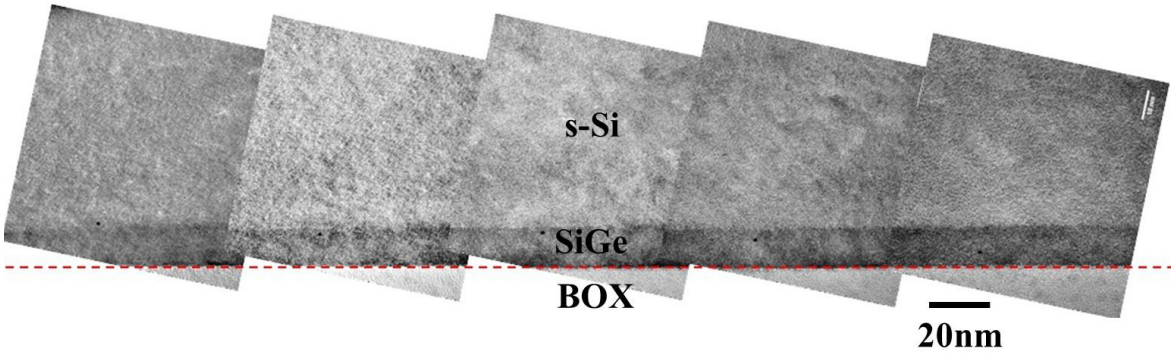

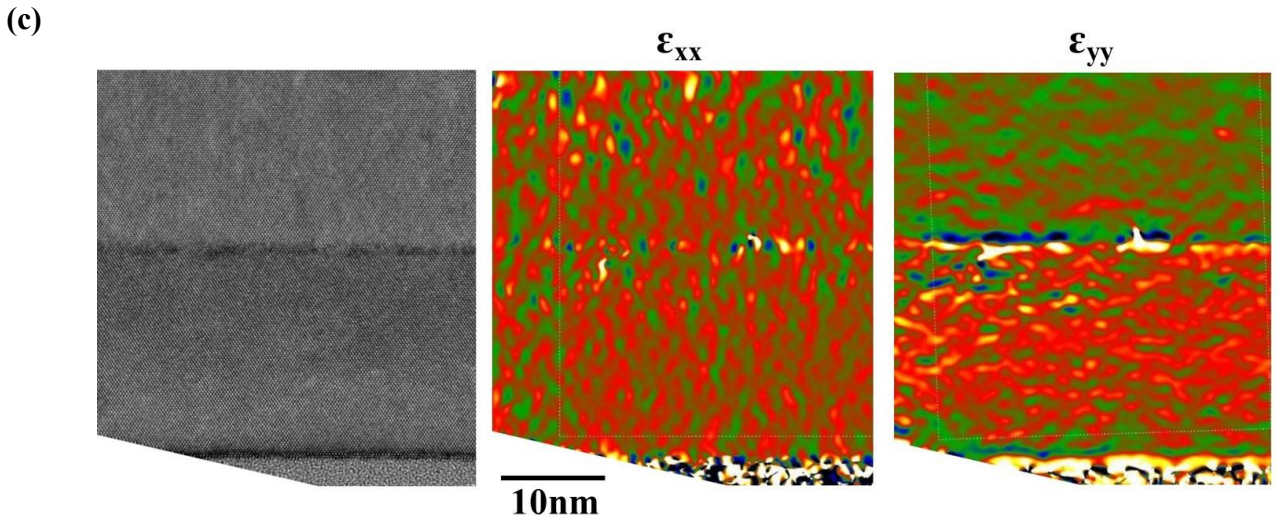

Figure 7: (a) Large-scale TEM image of the cross-section sample on which one can see the constituents of the device, from bottom to top: Si substrate, poly-Si, BOX, Si/$Si_{1-x}Ge_x$ and Pt cap layer; (b) HRTEM image of the Si/$Si_{1-x}Ge_x$/BOX system; (c) HRTEM reference image and GPA color-coded map of ε_{xx} ($\Delta a/a$) and ε_{yy} ($\Delta c/c$) in the *a*-*c*-directions.

To get a complementary insight on strain relaxation, we counted directly on the image the atomic distances and integrated the measurements on areas typically 1000 × 1000 pixels. The (002) interplanar distances measured are 2.738 Å for $Si_{1-x}Ge_x$ ($x \approx 0.2$) which corresponds to a fully relaxed layer and 2.692 Å (instead of 2.715 Å for bulk Si) which corresponds to a tensile strain of - 0.85 % in good agreement with the GPA measurements.

3.2 Simulations

The elastic theory is used to predict and explain the strain evolution of a Si film in epitaxy on $Si_{1-x}Ge_x/SiO_2$ substrate (Figure 1f), as a function of experimental parameters (Si/$Si_{1-x}Ge_x$ thicknesses and Ge concentration). We consider that during the epitaxy of Si, the $Si_{1-x}Ge_x$ film is rigidly fixed at its lower interface to the BOX, so that this film is held in its initial strain state before Si epitaxy. In our experimental conditions, after low temperature condensation, we perform an annealing at 970 °C which homogenizes the Ge concentration throughout the (Si + $Si_{1-x}Ge_x$) layer. At this temperature, the viscous flow of the BOX provides an efficient elastic relaxation without dislocation nucleation. Consequently, in the simulations, we impose

a displacement vector at the $Si_{1-x}Ge_x$/BOX interface which is zero with respect to the relaxed state. This condition introduces finite size effects compared to the semi-infinite layer where one imposes the displacement vector to be zero in the $z \longrightarrow -\infty$ limit.

We note $h_{tot} = h + e$ the total thickness, with h (e) the Si ($Si_{1-x}Ge_x$) thickness (Figure 1f). The Si free surface is located at $z = H(\boldsymbol{r})$, where $\boldsymbol{r} = (x,y)$. We use the theory of linear and isotropic elasticity where the strain ε and stress σ tensors are linearly related [45] thanks to the Young's modulus Y and Poisson's ratio ν that are supposed to be identical in the Si and $Si_{1-x}Ge_x$. Stress arises from the lattice mismatch between the film (Si) and the substrate ($Si_{1-x}Ge_x$), characterized by the misfit $m = 1 - a^f/a^s$, with $a^{f(s)}$ is the film (substrate) lattice parameter. In the following, we compute all strain vectors u with respect to a reference state defined with the substrate lattice parameter a^s. Mechanical equilibrium enforces the relation $\nabla \cdot \sigma = 0$ and the strain state is determined with the boundary conditions. The substrate lower surface is supposed to be rigid and is set at its relaxed lattice parameter, so that:

$$u(z = 0) = 0 \qquad (1)$$

This situation dramatically changes the strain state compared to the deposition on a crystalline softer or stronger substrate [46]; [47]. As usual, the top surface is supposed to be free of stress, $\sigma n(z = h_{tot}(r)) = 0$, while the film/layer interface is coherent so that $u(z = e^-) = u(z = e^+)$ and

$$\sigma n_z (z = e^-) = \sigma \cdot n_z (z = e^+)$$

In the case of a flat film, i.e. when $H(r) = h_{tot}$ is constant, we find the solution:

$$u_0 = \left(0,0, m\frac{1+\nu}{1-\nu}(z - e)\right)$$

in the Si film, while u_0 vanishes in $Si_{1-x}Ge_x$. This solution is associated with an elastic energy density $\varepsilon_0 = \frac{Ym^2}{1-\nu}$. Contrarily to the case where the lower layer surface is free of stress [48], in our current conditions, the flat film solution does not depend on the ratio e/h_{tot}, and there is no strain sharing between the film and the substrate.

When the film is modulated with a small corrugation, $H(\boldsymbol{r}) = h_{tot} + h_1(\boldsymbol{r})$, the displacement vector may be expanded at first order in the surface slope [49] as $u = u_0 + u_1$ where u_1 is conveniently found in Fourier space in the x and y directions, with a wave vector k. The solution of the mechanical equilibrium involves here both e^{kz} and e^{-kz} terms, both in Si and $Si_{1-x}Ge_x$ layers. Eventually, one finds $u_1(k)$ and the elastic energy density on the surface $\varepsilon = \varepsilon_0 + \varepsilon_1$ where ε_1 is given by

$$\varepsilon_1(k) = -2(1+\nu)\ \varepsilon_0 A_k(kh_{tot})kh_1(k), \qquad (2)$$

in Fourier space, with

$$A_k(x) = \frac{(3-4\nu)sh(2x)+2x}{(3-4\nu)ch(2x)+2x^2+\frac{1}{2}[1+(3-4\nu)^2]} \quad (3)$$

Note again that the finite size effects at first order depend here solely on h_{tot}. This result coincides with the large thickness limit $h_{tot} \to \infty$ in the semi-infinite substrate case (large $Si_{1-x}Ge_x$ thickness) [50] where $A_k = 1$. More interestingly, it also corresponds to the $s \to \infty$ limit of [47] describing a film/substrate system deposited on a crystalline soft substrate with a Young modulus $Y^{sub} = sY$. In our current situation (rigid interface) one finds that at low-k,

$$A_k(kh_{tot}) = \frac{kh_{tot}}{1-\nu} + O(kh_{tot}) \quad (4)$$

Consequently, $\varepsilon_1(k)$ is analytic and no longer singular as $|k|$ in the $k \to 0$ limit, contrarily to the usual elastic relaxation in the semi-infinite or soft cases. In particular, in the film/soft substrate (*fss*) case [46], [47], one finds $A_k^{fss} = 1/s + O(kh_{tot})$ that only renormalizes the elastic energy density $\varepsilon_1(k)$ by $1/s$ at low k·e elastic stress described by (2) may be relieved by the morphological evolution of the surface, as generically described by the Asaro-Tiller-Grinfeld instability [51], [52]. Mass conservation enforces the diffusion equation [53] $\partial h/\partial t = D\Delta_s\mu$ where D is a diffusion constant, and Δ_s, the surface Laplacian. The chemical potential μ is the sum of the elastic energy density and surface energy $\gamma(h)\kappa$, where $\gamma(h)$ is the surface energy and $\kappa = -(h_{xx} + h_{yy})$ the surface mean curvature. The h-dependence of the surface energy describes the wetting effects [49]. In epitaxial systems, it may be given by $\gamma(h) = [\gamma_f\, 1 + c_w e^{-h/\delta_w}]$ after inspection of atomistic results [54]. Given the solution for the elastic energy, one finds that a modulation of wave-vector k grows in the linear approximation as $h_1(k, t) = e^{ik\cdot r+\sigma t}$ with

$$\sigma(k, h_{tot}, h) = -\frac{c_\omega}{\delta_\omega^2} e^{-\frac{h}{\delta_\omega}} k^2 + A_k(kh_{tot})k^3 - k^4 \quad (5)$$

in units of the space and time scales $l_0 = \gamma_f/[2(1+\nu)\varepsilon_0]$ and $t_0 = l^4/D\gamma_f$. Due to the presence of both the wetting and the finite-size elastic effects, the growth rate depends both on h_{tot} and h.

The first striking outcome of this analysis is that even without wetting interactions ($c_w = 0$), the rigid substrate introduces a new critical thickness h_c^0 below which ($h < h_c^0$), $\sigma(k)$ is negative and the instability is inhibited. Indeed, when $c_w = 0$, the small-k expansion of σ is

$$\sigma = -\left(1 - \frac{h_{tot}}{h_c^0}\right) k^4 + O(k^6) \quad (6)$$

with

$$h_c^0 = 1 - \nu \quad (7)$$

in dimensionless units. A similar result was found in [53] in the case of a rigid substrate. It is noticeable that h_c^0 only depends on a combination of elastic and surface effects and results from the lowering of the elastic relaxation due to the rigid interface [55]. In our experimental conditions, the interface rigidity weakens the instability development below a given thickness. This inhibition is thence inferred to elastic relaxation inhibition (i.e. it is not the consequence of wetting interactions). Conversely, an increased softness promotes the instability as the elastic cost in a softer substrate (associated with the elastic relaxation) is lowered [46], [47].

Another limit concerns the semi-infinite case where $Si_{1-x}Ge_x$ is a very thick substrate ($h_{tot} \longrightarrow +\infty$) while the Si film has a finite thickness (h). In these conditions, if we consider wetting interactions ($c_\omega \neq 0$), there is another critical thickness below which the morphological evolution cannot occur (when wetting interactions are sufficiently damped to allow strain relaxation). It corresponds to the ATG instability (h_c^{ATG}) in presence of wetting where $h_c^{ATG} = \delta_\omega log\left(\frac{4c_\omega}{\delta_\omega^2}\right)$ [49]. In these conditions, A_k = 1 and we find that below h_c^{ATG}, $\sigma(k)$ is always negative, while above h_c^{ATG}, $\sigma(k)$ displays a range of wave-vectors where it is positive, so that a morphological instability can grow.

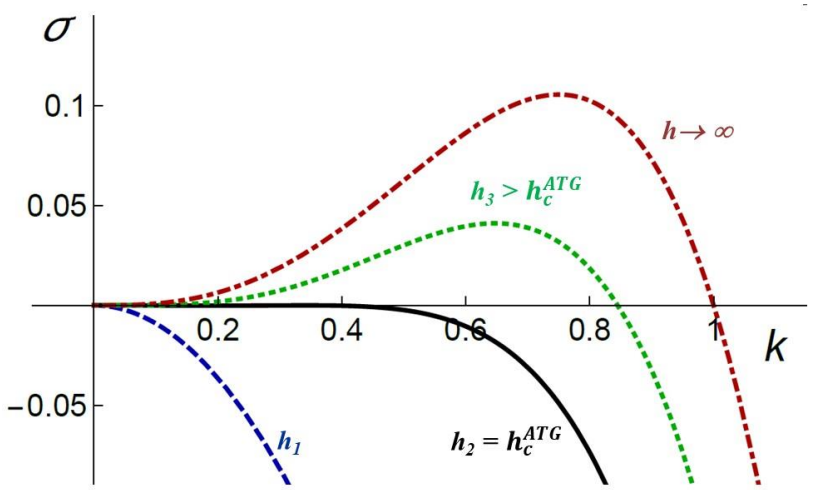

Figure 8: Growth rate of the elastic instability as a function of its wavevector k for a given layer thickness e and for $h_1 < h_c^{ATG}$ (dashed blue line), $h_2 = h_c^{ATG}$ (solid black line), $h_3 > h_c^{ATG}$

(dotted green line) and in the h → + ∞ limit (dash-dotted red line). The length and time scales are l_0 and t_0. We choose $c_\omega = 0.1$, $\delta_\omega = 0.01$, ν = 0.273, a given e = 1 − ν, while $h_1 = 0.07$, $h_2 = 0.116$ and $h_3 = 1$.

In the general case, with both wetting interactions and a finite thickness h_{tot}, one finds a Stranski-Krastanov like behavior (Figure 8). Below the h_c^{ATG} critical thickness, that a priori depends on the layer thickness e, the growth rate is negative and the instability is inhibited (h_1). The Si film remains fully strained and flat. Conversely, for $h > h_c^{ATG}$, the instability grows and strain relaxation spreads through the Si film (h_3). h_c^{ATG} has two major specificities, first it depends only on e as a result of the combination of both the elastic inhibition and wetting interactions and second, its value is of the order of the instability length scale l_0 which is of the order of hundreds of nanometers in our experimental conditions, well above the Si thickness (70 nm) deposited for the targeted device. The typical dependence of $h_c(e)$ is plotted in Figure 9. When $e \rightarrow +\infty$, h_{tot} also diverges and the instability growth rate coincides with the semi-infinite substrate case ($h_c(e) \rightarrow h_c^{ATG}$). On the contrary, when $e \rightarrow 0$, $h_c(e)$ nearly coincides with $h_c(e) \approx h^0 - e$. In between these two limits, ($0 \leq A_k \leq 1$ for $\nu \leq ½$) $\sigma(k, h_{tot}, h)$ (and strain relaxation) is always much reduced compared with the normal ATG situation. In presence of wetting interactions, $\sigma(k, h_{tot}, h)$ is even lower than without wetting interactions, and the instability only develops when $h_{tot} \geq h^0$ with $h_c(e) \geq h^0 - e$ which in our experimental conditions correspond to 83 nm (for x = 0.2 and e = 19 nm)

As a conclusion, the calculations show that strain relaxation will occur when $h_c(e) \geq \sup(h_c^{ATG}, h^0 - e)$. This condition is indeed satisfied in the numerical solution for $h_c(e)$ plotted in Figure 9.

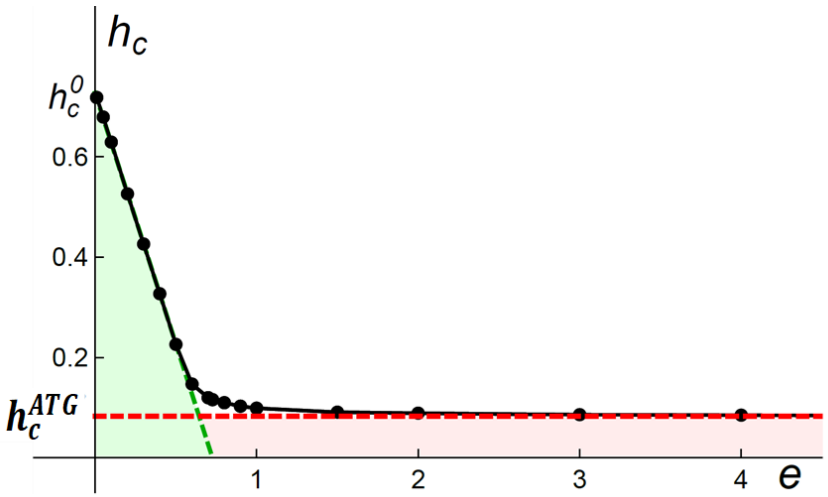

Figure 9: Numerical solution for $h_c(e)$ above which the instability grows, as a function of the layer thickness e, with the parameters described in Figure 8 and in units of l_0.

3.3 Discussion

During this study we blew out crucial locks that were blocking the fabrication of Si. First the strain relaxation of $Si_{1-x}Ge_x$ (SGOI) which must be achieved without change of the uniformity and flatness and without dislocation nucleation. In these layers, strain relaxation commonly occurs by the introduction of 60° perfect dislocations or planar defects, such as microtwins and stacking faults that are associated with loss of coherency during oxidation/annealing. In addition to this extended defect mechanism, the buckling of thin SGOI films has been demonstrated as another mechanism which explains the discrepancy between thermodynamically predicted strain levels and experimental results [56]. When the system is deposited on a SiO_2 viscous layer, the buckling rate of the SGOI film (i.e. the inverse of the bucking time constant τ_B) can be expressed using the Föppl von Kármán plate equation which describes the large deflection of thin compressed films with:

$$\frac{1}{\tau_B} = \frac{E}{12\eta(1-\eta^2)}\left[\frac{sinh\left(2h_{SiO_2}k\right) - 2h_{SiO_2}k}{1 + cosh\left(2h_{SiO_2}k\right) + 2\left(h_{SiO_2}k\right)^2}\right] \times [12e(1-\nu)ek - (ek)^2]$$

where η is the viscosity of SiO_2, h_{SiO2} the thickness of SiO_2 and k the wavenumber of a particular buckling mode [56]. In these conditions, the relaxation of SGOI strain, below the glass transition temperature (≈ 1100 °C) has the same activation energy as viscous flow and is controlled by the viscosity [57] which varies with temperature following an Arrhenius relation. In our experimental conditions, after low temperature condensation (800 °C), $Si_{1-x}Ge_x$ layer (x=0.4 and $h_{Si1-xGex}$ ≈ 12 nm) is fully strained on SOI (as already reported [38] [39]). The critical step is then to transform this fully strained Ge rich layer into relaxed SGOI (preferably fully relaxed). In addition, as deduced from the simulations, $Si_{1-x}Ge_x$ should have low thickness and concentration to avoid elastic strain relaxation (since $h_c(e)$ and x are directly related). For the targeted device, the layer should also be homogeneous in concentration, flat (no buckling), and free of dislocation. The results show that at a very crucial temperature annealing (T ≈ 950 °C) both homogenizing of the concentration throughout (Si + $Si_{1-x}Ge_x$) and strain relaxation are optimal. It provides the fabrication of a perfectly flat $Si_{1-x}Ge_x$ template layer with x = 0.23 % and e ≈ 20 nm. In addition, at this temperature (i.e. below the glass transition temperature), SiO_2 has a low viscosity which could allow a slow layer by layer redistribution of $Si_{1-x}Ge_x$ slightly pushing SiO_2 in a planar way which would provide elastic strain relaxation without buckling [58]. The annealing is also very efficient to flatten the $Si_{1-x}Ge_x$/BOX interface. The temperature of annealing is here very crucial since at lower temperature, strain is not relaxed (SiO_2 is too rigid) while at higher temperature, there is nucleation of dislocations.

The second tricky step is the epitaxy of Silicon which should lead to expitaxial Si, fully strained on $Si_{1-x}Ge_x$. As demonstrated by elastic theory, epitaxy should be performed at low enough temperature (500 °C) to have a rigid $Si_{1-x}Ge_x$/BOX interface and avoid strain sharing, as reported in the simulations. Indeed, strain sharing is forbidden only when the interface is rigid. It is roughly explained by the energy cost (when the interface becomes very rigid) to relax strain at this interface which becomes too large as compared to the gain of relaxation energy. In addition, the simulations also show that *e* should be lower than the critical thickness $h_c(e)$ where corrugation development starts as a consequence of Si strain relaxation (Figure 8). We have shown that it is the combination of all these very specific parameters chosen on the basis of elastic simulations that allow to get the fully strained Si layer as demonstrated here.

4. Conclusion

Thanks to a multi-disciplinary approach based on elastic modelling and series of highly specialized experiments, we have developed a simple process for engineering tensile strained Si layers on a relaxed SGOI film using parameters precisely fitted to theoretical predictions. Contrary to the previous processes reported in the literature, the present method allows to fabricate defectless layers thanks to a fine tuning of experimental parameters: $Si_{1-x}Ge_x$ composition and thickness and temperatures of epitaxy, condensation and annealing. The three crucial steps are: (i) fabrication of ultra-thin Ge rich $Si_{1-x}Ge_x$ layer by low temperature condensation, (ii) relaxation and homogenization of SOI/Ge rich $Si_{1-x}Ge_x$ layer during annealing without dislocation nucleation nor buckling. Elastic relaxation results from the low BOX viscosity at high temperature, which would promote a slow layer by layer $Si_{1-x}Ge_x$ matter redistribution (iii) Si epitaxy without strain sharing, producing defect-free, planar and fully strained Si. Elastic simulations show that inhibition of strain sharing is only made possible if $Si_{1-x}Ge_x$ buffer layer is thin and rigidly fixed to the BOX. The process reliably and reproducibly produces a Si layer under - 0.85 % tensile strain. According to the literature, such tensile strain should lead to 110 % increase of the electron mobility, and thus significantly decrease the Ron*Coff figure of merit of RF-switches. The developed process is applied to the pilot large multifinger 2.5 V n-type MOSFET on SOI used for RF-switches applications of XFAB. The electrical characteristics foreseen place it at the top level of the components made in the world. The developed process is simple and generic and can be adapted to many other devices.

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Author Contributions

I.B. and G.U. conceived the project; I.B., N.P., F.D. and G.U. conceived and designed the experiments and supervised the work, T.D. performed the MBE experiments, T.D. and L.F. performed TEM experiments and GPA analyses. L.F., M.A., A.R. and I.B. interpreted the results,

J.N.A. developed the theoretical model and made the calculations. All authors contributed to the scientific discussions, manuscript preparation, and final revision. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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[55] Note: see the vanishing of Ak at low-k given in (4), as opposed to the semi-infinite substrate case where Ak = 1.

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