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Solar Energy

GaAsP/SiGe tandem solar cells on porous Si substrates

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GaAsP/SiGe Tandem Solar Cells on Porous Si Substrates

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Abstract

III-V compound semiconductors and SiGe alloys can be combined to develop multijunction solar cells on Silicon substrates with optimum bandgap combinations. Current implementations of such devices have reached efficiencies over 20%, using thick –and thus costly– buffer layers which induce the appearance of cracks in large area samples. As a strategy to mitigate these two issues (thick buffers and cracking), a GaAsP/SiGe tandem solar cell has been developed employing group IV reverse graded buffer layers grown on Ge/Si virtual substrates with a subsurface Silicon porous layer. Reverse buffer layers facilitate a reduction in the threading dislocation density with limited thicknesses but can also induce cracks. To minimise this, a porous silicon layer has been incorporated close to the Ge/Si interface so that the ductility of this layer suppresses crack propagation. In terms of solar cell performance, this porous layer reduces the problem of cracks, not totally supressing them though. Accordingly, the low shunt resistance observed in previous designs has been increased thus improving solar cell efficiency, which is still notably behind designs using thicker forward graded buffer layers. The first results of this new architecture are presented here.

Keywords: III-V on silicon, GaAsP/SiGe, porous silicon, reverse buffer layers, tandem on silicon.

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1. Introduction

III-V multijunction solar cells are very efficient, repeatedly breaking conversion records in recent years (Geisz et al. 2020), but still expensive for terrestrial applications. Conversely, silicon solar cells whose technology dominates the terrestrial market (Battaglia et al. 2016) are approaching a standstill having essentially reached their practical efficiency limit (Yoshikawa et al. 2017). Therefore, the integration of III–V semiconductors on silicon substrates has been the target of numerous research lines from the 1980s (Suzuki et al. 1991, Hayashi et al. 1994a) based on the premise of high performance III–V semiconductor multijunction solar cells combined with the low-cost advantages of large area silicon substrates (Hayashi et al. 1994b, Kurtz et al. 2008, Supplie et al. 2018, Essig et al. 2017). Other alternatives for Si-based tandem solar cells have been proposed as perovskites on Si (Leijtens et al. 2018), or thin films on Si (Ramanujam and Singh 2017, Valentini et al. 2019), to name the most relevant. Recently, perovskites on Si have achieved higher efficiencies than III-V/Si architectures exceeding 29% (Al-Ashouri et al. 2020) as compared to 25.9% for the best device reported with III-V/Si (Feifel et al. 2021). However, the limited reliability and durability of perovskites (Wu et al. 2019) in contrast to III-Vs (Nuñez et al. 2021) is a big hurdle for their industrial deployment, which makes the research on III-V/Si design a solid alternative.

Among the wealth of approaches to combine III–V materials and silicon for PV applications, monolithic structures are of particular interest for their straightforward integration in current manufacturing lines and lower production cost than other approaches. In this monolithic integration III-V and group-IV compounds are grown heteroepitaxially on a single substrate to produce a multijunction solar cell, which is then processed as a monolithic device, i.e. forming metallic contacts both at the front and rear and depositing an antireflection coating. However, the direct growth of III–V and group-IV semiconductors on silicon must tackle key difficulties such as the large differences in lattice parameter, thermal expansion coefficients or polar on non-polar growth. Therefore, smart engineering of the buffer layer between the silicon and the III–V layers is essential in order to accommodate these dissimilar parameters.

III-V/Si architectures have been demonstrated for optoelectronics with lasers (Groenert et al. 2003), bipolar transistors (Lew et al. 2007), photodetectors (Luan et al.

1999) or light emitting diodes (Yang et al. 2002). As for monolithic III-V/Si photovoltaic devices, GaAsP/Si dual junctions using GaP buffer layers (Hayashi et al. 1994a, Lepkowski et al. 2020, Fan et al. 2020a, Fan et al. 2020b, Fan et al. 2019, Caño et al. 2021, Saenz et al. 2020), GaInP/GaAs tandem cells on Ge/Si virtual substrates (Ginige et al. 2006, Wang et al. 2017, Kim et al. 2018, Bioud et al. 2019, García et al. 2021) and GaAsP/SiGe dual junctions grown on inactive Si substrates have been developed (Schmieder et al. 2012, Pitera et al. 2011). In the latter design, an extra degree of freedom for bottom cell bandgap tunability is provided by changing the composition of the SiGe alloy. A further step ahead is the addition of minute amounts of tin to form SiGeSn alloys, which provide both bandgap and lattice constant adjustability, at the price of having to sort out big difficulties in material growth and quality (Roucka et al. 2016, Soref and Perry 1991). Anyhow, $Si_{1-x}Ge_x$ alloys allow a reasonable approach to the optimum bandgap combination for a dual-junction solar cell (Connolly et al. 2014). Actually, the ~0.95 eV-subcell for an ideal current matching in 3- and 4-junction solar cell designs can be achieved with $Si_{1-x}Ge_x$, with x~70-80%. (Friedman et al. 2002). Moreover, SiGe alloys have reached a significant level of maturity in terms of material growth and quality, since they are used in the electronic industry for the fabrication of bipolar transistors, MOS transistors, CMOS and BiCMOS technologies (Haddara et al. 2017). In fact, GaAsP/SiGe tandem cells on Si have reached efficiencies over 20% (Wang et al. 2016, Pitera et al. 2011, Conrad et al. 2018). In these structures, a $Si_{1-x}Ge_x$ buffer is grown on the silicon substrate as a graded layer, increasing Ge content until the desired Ge composition is reached (Fitzgerald et al. 1992, Wang et al. 2016, Faucher et al. 2013, Conrad et al. 2016). The thickness of such buffer layers is typically between 5 and 15 μm in order to reduce the threading dislocation density and achieve the target bandgap (defined by the lattice parameter) while retaining sufficient quality in the surface morphology (Schmieder et al. 2012, Groenert et al. 2003, Faucher et al. 2013, Wang et al. 2016). Accordingly, following the terminology coined by Shah and co-workers (Shah et al. 2008, Capellini et al. 2010), we will refer to this kind of graded buffer layer as a forward-graded buffer.

Here, an innovative architecture for the integration of III–V compounds and SiGe alloys on silicon substrates is presented, using so-called reverse-graded buffers (Shah et al. 2008, Capellini et al. 2010). This III–V/SiGe/Si approach is aggressive in terms of

growth; a germanium layer is directly grown by CVD on the silicon substrate, despite the large lattice mismatch, utilizing a growth scheme that has demonstrated dislocation densities as low as $5x10^6cm^{-2}$ (Lee et al. 2016). Then, a $Si_{1-x}Ge_x$ graded buffer layer is grown, decreasing from pure Ge to the desired final target (Ge ~75%). Because of the almost complete relaxation of the initial Ge layer and the reduction in lattice constant with increased silicon content, reverse-graded buffers are subject to tensile strain. The tensile strain facilitates the movement of glissile threading dislocations, aiding their annihilation. Reverse-graded buffers thus offer promise for both lower TDD and smoother surfaces (Xie et al. 1994, Capellini et al. 2010). Furthermore, for Ge contents over 50%, reverse-graded buffers are thinner due to the smaller change in composition that is needed, which decreases costs (Shah et al. 2008, Ward et al. 2014). On the other hand, the high tensile strain and the larger differences in thermal expansion coefficients can result in the appearance of cracks (Shah et al. 2010) that cause a degradation in the device performance, as we have shown in a previous work (Caño et al. 2020). In fact, the differences in thermal expansion coefficients in the buffer layer itself is lager in reverse buffers than in forward buffers, due to the abrupt change between Si and Ge.

As way to sort out some of the aforementioned problems, in this new architecture, a porous silicon layer on the substrate subsurface has been implemented. Porous silicon has been previously used in optoelectronic (Zheng et al. 1992, Tsai et al. 1993) and PV applications (Smestad et al. 1992, Jiménez-Cruz et al. 2018) as window layers, passivation or anti-reflection coatings (Menna et al. 1995, Prasad et al. 1982). Here, the porous silicon layer is used to absorb strain energy due to its lower stiffness compared to bulk silicon (Menna et al. 1995, Barla et al. 1984), since it has lower Young's modulus (Karbassian 2017). This way, we think that the Si/porous-Si structure should behave similarly as a partially compliant substrate (Ayers 2008).

In order to understand the potential of reverse buffer layers in the context of III-V/Si multijunction solar cell development, we herein present the results of GaAsP/SiGe tandem solar cells grown on silicon substrates with porous layers. In this paper, we report the characterization of these structures and solar cells, highlighting the issues that arise and comparing them with tandem GaAsP/SiGe devices grown on standard silicon wafers from our previous works (Caño et al. 2020).

2. Experimental

Fig. 1 shows the structure of the solar cells in this study with doping levels and thicknesses. The samples were grown following a combined approach using both chemical vapor deposition (CVD) and molecular beam epitaxy (MBE). Firstly, porous silicon was created by means of electrochemical etching on 6-inch (100) 6º off towards [110] silicon wafers with a resistivity of 0.01 Ωcm. Then, all group-IV layers were grown in an ASM Epsilon LPCVD reactor at a temperature of ~650 °C using standard precursors (SiH_4 and GeH_4 for the alloys and boron and phosphorus for the p-type and n-type doping respectively). An initial 3.5 µm germanium layer was grown directly on the silicon wafer followed by a ~1.5 µm SiGe reverse-graded buffer, changing composition gradually from pure germanium to 76% Ge. Afterwards, the $Si_{0.24}Ge_{0.76}$ bottom cell with E_g ~1 eV was grown. Before the transfer to a Veeco Gen2000 MBE reactor, the $Si_{0.24}Ge_{0.76}$ bottom cell was capped with a 5 nm Ge layer in order to prevent oxidation of the Silicon in the SiGe, which is difficult to remove thermally in the MBE chamber. In the second growth III-V layers were grown lattice matched to the $Si_{0.24}Ge_{0.76}$ bottom cell, forming the tunnel junction and the $GaAs_{0.75}P_{0.25}$ top cell (E_g ~1.65 eV) (Pitera et al. 2011, Wang et al. 2015, Diaz et al. 2015) at ~650 °C with a growth rate of ~1 µm/h. In our previous work on conventional Si substrates, the growth was carried out under similar conditions. High-resolution X- ray diffraction reciprocal space maps (RSMs) of the structures were obtained using an X'Pert Pro MRD tool.

An important remark about this structure should be made at this point. As shown in Fig. 1, the SiGe bottom cell is just 1 µm thick. This value is far from the ~5-6 µm needed for a current matched device, so our solar cells will be severely bottom cell limited. This design decision was made to minimize the risk of epilayer peel-off during the processing of the solar cells, which can be a consequence of the inclusion of porous silicon. In our experience, the handling of large area (6 inch) wafers with thick epilayers is not easy. Oftentimes, minor shocks during the manual handling of the wafers cause the epilayers to peel off catastrophically, ending up shattered into a thousand pieces. To minimize this risk, we limited the thickness of the bottom cell to one micron. Therefore, the goal of this study is an initial assessment the joint use of porous silicon layers and reverse graded

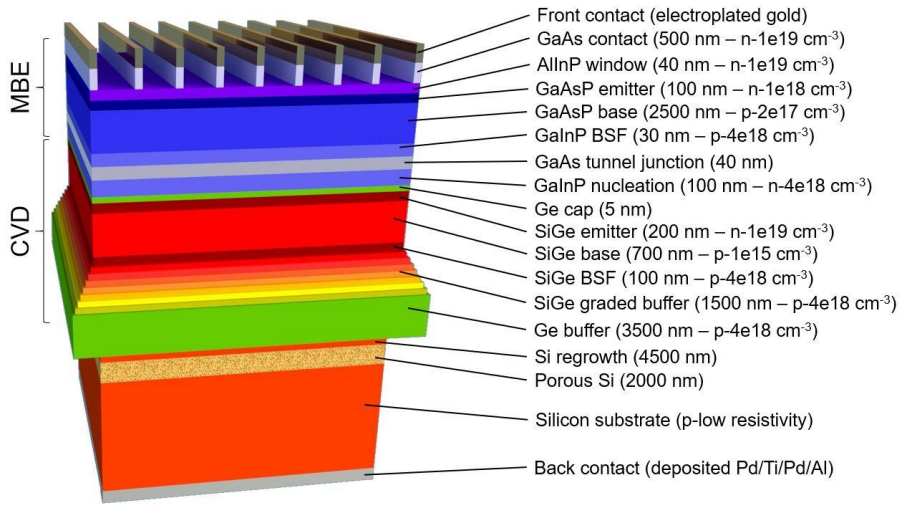

FIGURE 1. Structure of the GaAsP/SiGe tandem with porous silicon buffer layer, where the lattice constants are schematically represented. Layers with thicknesses and doping levels are labeled.

buffers to implement functional GaAsP/SiGe tandem solar cells rather than the achievement of a high efficiency which is out of reach with a severe current mismatch.

The epi-wafers were processed into ~0.10 cm^2 (3.2 mm × 3.1 mm) solar cells with conventional photolithography techniques. Since group-IV and III-V semiconductors have different processing requirements, both front and rear contacts were specifically designed to reduce thermal budget. In this way, the high temperatures of conventional silicon metallization were avoided, minimizing the risk of crack propagation and

guaranteeing material compatibility. The front contact was formed using electroplated gold (~600 nm thick) without any alloying. The rear contact was deposited with Electron Beam Physical Vapor Deposition (EBPVD) and consisted of a stack of Pd(50nm) / Ti(50nm) / Pd(50nm) / Al(1000nm) alloyed at 170ºC for 600 s. No antireflection coating (ARC) was deposited on the cells. The devices were isolated though mesa etching using a $NH_4OH–H_2O_2–H_2O$ (2:1:10) solution for arsenides. This solution is also suitable for etching SiGe. In the case of phosphides, $HCl–H_2O$ (1:1) was used to remove them.

After device fabrication, External Quantum Efficiency (EQE) was measured using a custom-made tool based on a 1000W Xe lamp, a triple-grating monochromator (JOBIN-YVON) and a lock-in amplifier. I-V curves were measured using the four-probe method with a Keithley 2602 source-meter instrument and a home-made AAA solar simulator based on a 1000- W Xe- lamp and an ORIEL 68820 stabilized power supply. Capacitance-voltage (C-V) measurements were carried out with an HP 4284 LCR meter. Curves were collected with a 5 mV signal at 30 kHz, which is considered to be high-frequency (Recart and Cuevas 2006). Spectral Photovoltage (SPV) measurements were performed in two-probe contact mode at room temperature using a 200W QTH-lamp filtered through a 1/8 monochromator (Oriel) as probe beam and a lock-in amplifier (Stanford).

3. Results and Discussion

3.1 Material Characterization

A cross-section of the whole structure can be observed in the Transmission Electron Microscopy (TEM) image in Fig. 2, where the most relevant layers in the structure have been identified. The thicknesses of the layers agree well with the nominal values in Fig. 1. As can be seen, the porous silicon layer is clearly delineated between the underlying substrate and overlying CVD-grown Si. The other group-IV layers have sharp and flat interfaces. Nonetheless, the interface between the SiGe subcell and the GaAsP top cell shows some unevenness, which is even more noticeable at the GaAsP/GaAs interface, which is especially susceptible to defects (Sharma et al. 2013). This can be observed in figure 3, which shows TEM images of key parts of the structure at higher magnification. Fig. 3.a shows the porous layer with a range of pore sizes, delimited by a line of large pores at the substrate interface. As discussed below, this may impact the series resistance

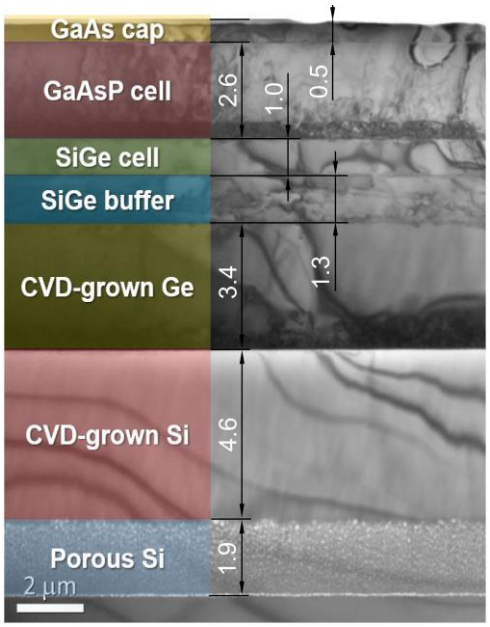

FIGURE 2. Cross-sectional bright-field transmission electron microscope image of the as-grown GaAsP/SiGe wafer, with key layers identified. The layer labeled GaAsP cell includes the tunnel junction and nucleation layer. The labels on the right indicates which layers are shown in figure 3.

of the cell. Fig. 3.b shows group IV layers including the Ge layer, the SiGe reverse buffer and the SiGe bottom subcell. The Ge/Si interface is very defective (as expected) but most dislocations are confined to the vicinity of the interface. In the SiGe reverse graded buffer, the interfaces between the steps are also delineated by misfit dislocations. Figure 3.c shows the GaAsP top cell and the GaAs cap layer, while Fig. 3.d shows a detail of the IV/III-V interface. In both figures the GaAsP layers appears very defective, with an irregular interface with bumps and voids, and with defects –both dislocations and microtwins– propagating upwards from the defective interface.

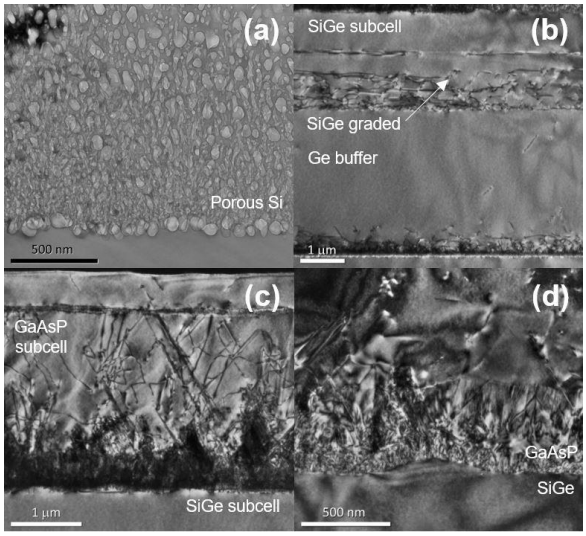

FIGURE 3. Cross-sectional TEM images of some details of the structure in Fig. 2. (a) bright-field 004 image of the porous layer; (b) dark-field 220 image of the Ge/SiGe graded buffer/ SiGe subcell; (c) dark-field 220 image of the GaAsP subcell; (d) dark-field 220 image of the GaAsP interface.

Figure 4 shows X-ray RSMs from symmetric 004 (a) and asymmetric 224 (b) reflections of the complete structure. The different layers in the structure can be identified and their lattice mismatch and composition quantified. All the layers were found to be fully relaxed. The silicon substrate peak is clearly visible in the upper left part of the graph. The Ge buffer peak can be observed with a mismatch of 4.36%, as deduced from the maps. Then, the diffracted intensity from the SiGe graded buffer layer spreads from the Ge peak to the SiGe bottom cell peak, with a composition of $Si_{0.24}Ge_{0.76}$. The $GaAs_{0.75}P_{0.25}$ layers grown on top are found to be slightly lattice-mismatched, which could be contributing to the poor quality of these layers. In fact, these III-V semiconductor layers (GaAs contact and GaAsP top cell) show a lower crystallographic quality, as indicated by their high peak FWHM, consistent with was observed in Figs. 3.c and 3.d. The threading dislocation density (TDD) of the full structure could not be measured. However, the cross section TEM images shown (Fig. 3.c) indicate a high value. Concerning the SiGe bottom cell, in a previous work where similar structures

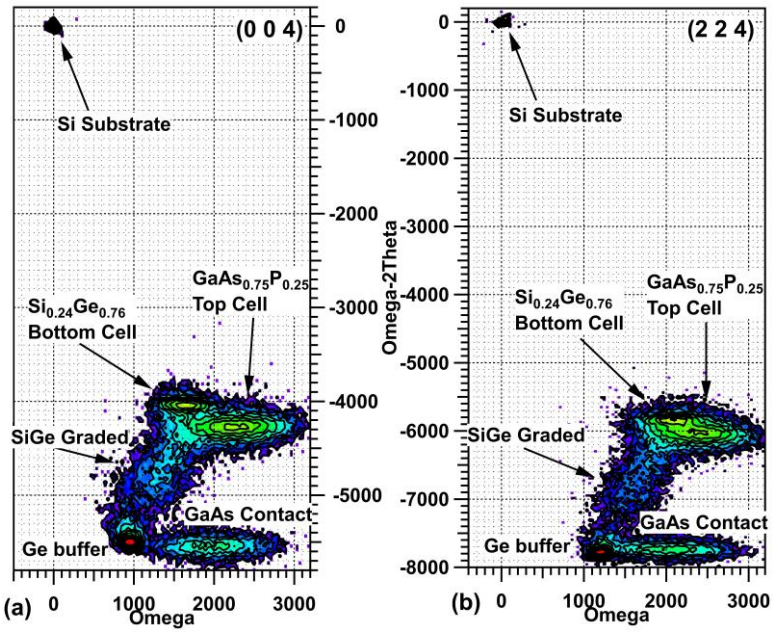

FIGURE 4. Reciprocal space maps (RSM) of the structure, including (004) reflections (a) and (224) reflections (b)

were grown on standard silicon wafers, a TDD of ~$8x10^5$ cm^{-2} was measured (Caño et al. 2020). This level is comparable to TDDs reported in other studies of forward buffers in $Si_{1-x}Ge_x$ with x ~80% (Ringel et al. 2002, Groenert et al. 2003, Milakovich et al. 2015) and thus suggests that the challenge of these structures relies more on the optimization the epitaxial growth conditions for porous silicon substrates rather than the use of reverse graded buffers.

On the wafer surface, some cracks are still visible to the naked eye, although the crack density has been qualitatively reduced as compared with growths on standard Si substrates with equally thin bottom subcells (Caño et al. 2020). The precise quantitative assessment of the cracking density is still an open question. We observe that the cracking is very irregular amid wafers of the same batch and even in different areas of the same wafer. Even more so, we have evidence that apparently clean areas have buried cracks that only appear when the upper layers are etched-off. For these reasons, the precise crack density could not be quantified and remains under investigation.

3.2 Solar Cell Results

Fig 5.a shows in red the experimental External Quantum Efficiency (EQE) of the top cell in the GaAsP/SiGe solar cells grown on porous Si substrates. The EQE of a solar cell with the same structure –i.e. also with a thin 1 µm SiGe bottom cell– but manufactured on standard Si wafers is included for reference. The final tail of the EQE (E_g ~1.64 eV) agrees well with the $GaAs_{0.75}P_{0.25}$ composition determined from the reciprocal space maps, which should correspond to around E_g = 1.66 eV. However, the EQE reaches a maximum of ~50% whereas other works in the literature for similar devices grown by MBE report clearly higher EQEs, as can be observed in the green line corresponding to GaAsP solar cell grown by Grassman and coworkers on Si with GaP nucleation layers and GaAsP graded buffers (Grassman et al. 2016). We choose to benchmark our results with (Grassman et al. 2016) since the GaAsP top cell has a similar structure – though with a slightly higher bandgap – also grown by MBE and underwent a reactor transfer prior to the growth of the top cell. There are better results in the literature (Fan et al. 2019, Diaz et al. 2015, Grassman et al. 2019) that we do not use as

a benchmark simply because they were either grown with notably different structures or techniques (MOVPE), or lack sufficient structural information.

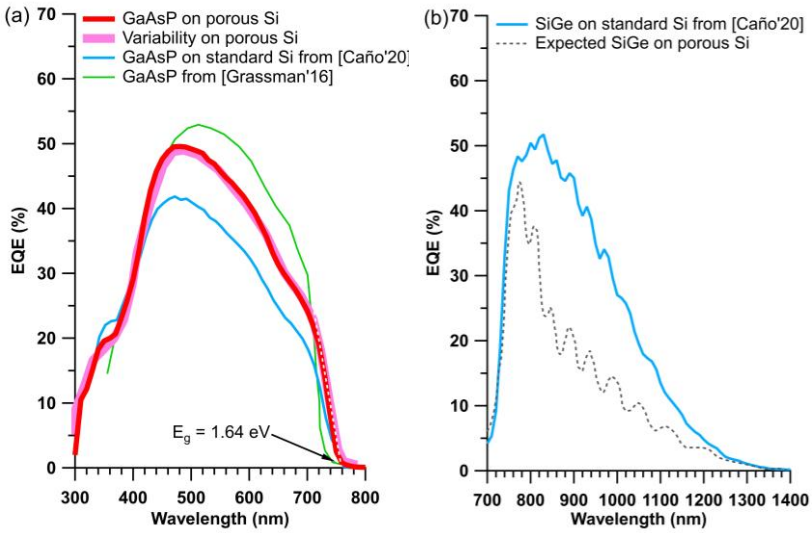

FIGURE 5. Experimental EQEs of the GaAsP/SiGe tandem solar cells on porous silicon in comparison with other results from the literature. (a) Experimental EQE of the best GaAsP cell grown on porous silicon (thick red line); thin pink lines represent the EQE of other devices in the same wafer to give an idea of performance homogeneity; a linear fit to obtain the bandgap has been included as a dashed line; EQE of the best GaAsP top cell grown on standard silicon wafers (blue line) (Caño, Pablo et al. 2020); EQE of a GaAsP top cell taken from (Grassman, T. J. et al. 2016) as a benchmark (green line). (b) Experimental EQE of the SiGe subcell grown on standard silicon wafers (blue line) (Caño, Pablo et al. 2020); expected EQE of SiGe bottom cell grown on porous Si substrates estimated from previous simulations (Caño et al. 2020) and Hovel's equations (Algora and Rey-Stolle 2016).

Fig. 5.b shows in a black dashed line the expected (i.e. simulated) EQE from the SiGe bottom cell that could not be actually measured. In our previous work, the EQE of 1 µm thick SiGe bottom subcells could not be measured either. However, as shown in a blue line in Fig. 5.b, the EQE of thicker SiGe subcell designs (5 µm) could be measured and thus a functional GaAsP/SiGe tandem solar cell on silicon was demonstrated (Caño et al. 2020). However, in the structure grown on porous Silicon only the top cell EQE could be measured, even though many solar cells were manufactured and tested. The lack of bottom cell response will be discussed later.

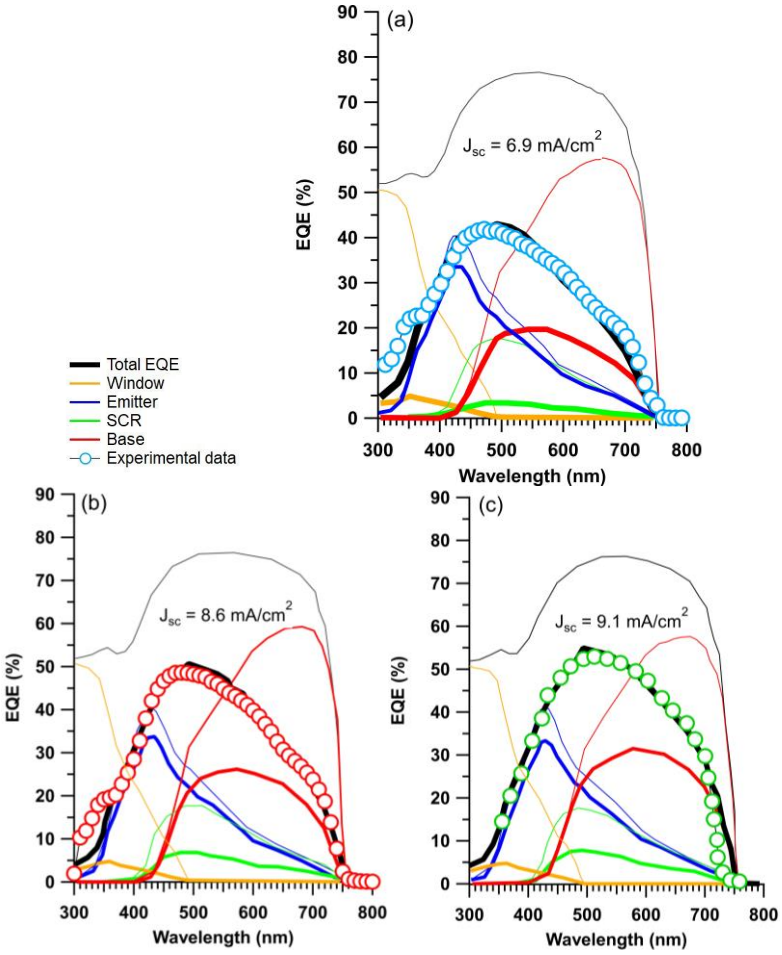

FIGURE 6. Simulated EQEs of the GaAsP/SiGe tandem solar cells on porous silicon in comparison with other results from the literature. (a) Simulation of the EQE of the GaAsP to cells in GaAsP/SiGe tandems grown on standard Si substrates, (taken from (Caño et al. 2020)). (b) Simulation of the EQE of the GaAsP to cells in GaAsP/SiGe tandems grown on porous Si substrates (this work); (c) Simulation of the EQE of the GaAsP to cells in GaAsP/Si tandems (taken from (Grassman et al. 2016)). Round symbols correspond to the experimental data. The thick black line is the total simulated EQE whereas the thin black line corresponds to total absorptance. The thick colored lines correspond to the contributions of each layer: orange for the window, blue for the emitter, green for the space charge region and red for the base. The thin colored lines are the absorptance in each layer with the same color code. The J_{SC} obtained from the integration of the experimental EQE over the AM1.5G spectrum is included in each graph.

In order to gain some insight into the performance differences of the top cells, EQE simulations were made using an analytic model (Algora and Rey-Stolle 2016). Figure 6 present the results of these simulations for GaAsP subcells grown on: standard Si (Fig. 6.a) (Caño et al. 2020); porous Si (Fig. 6.b) (this work); and our reference device from

the literature (Fig. 6.c) (Grassman et al. 2016). In these figures, circles correspond to the experimental data of Fig. 5.a and lines account for the modelling. The thick black line in each panel is the calculated total EQE whereas each thin black line corresponds to the total absorptance in the top cell (i.e. the ideal EQE with unity collection efficiency). Thick colored lines correspond to the contributions of each layer with the color code as indicated in the figure caption, whereas their thin counterparts again correspond to the absorptance in each layer. Therefore, the difference between thick and thin lines of the same color gives a visual indication about how close (or far) a layer is from perfect collection efficiency. Comparing the calculated EQE with the absorptance, it can be concluded that the response of all GaAsP top cells clearly shows room for significant improvement. In the case of the emitter (blue lines), very similar responses are found in the three designs. In all cases it could be fitted with a diffusion length of ~100 nm, which coincides with the emitter thickness in the three cases. In fact, this yields a reasonable blue response of the three devices. However, the base and space charge region are clearly different in the three designs. The response of the base is some way below the corresponding absorptance curve (thin red lines). In addition, the three designs behave quite differently: we see a remarkably low response in the cells grown on standard Si (Fig. 6.a), which could be fitted with a diffusion length of ~200 nm; there is a very low response in the cells grown on porous Si (Fig. 6.b), which could be fitted with a diffusion length of ~350 nm; and we find a low response in the cells from (Grassman et al. 2016) (Fig. 6.c), which could be fitted with a diffusion length of ~550 nm. In all three cases, the diffusion lengths are notably smaller than the base layer thickness (2 μm) and thus the collection efficiency is deleteriously affected. Regarding the space charge region, some differences in collection efficiency are observable too. In each case, it was necessary to simulate the space charge region (SCR) with a collection probability similar to that of the quasi-neutral base in order to obtain a reasonable fit of the experimental curve. If unity collection efficiency was assumed for the SCR (as in Hovel's equations (Algora and Rey-Stolle 2016)), no fit was possible.

Since the three GaAsP top cell structures are very similar, these simulation results can be understood as progress towards a better crystallographic quality in each design, though still reaching far from perfect minority carrier collection in the SCR and base. Other than the evident effect of TDD, it has been reported that the GaAsP epitaxial

growth conditions influence material quality in a poorly understood way (Fan et al. 2019). We therefore believe that there is an ample margin for improvement of these results by tuning the growth conditions, considering that this is our first attempt to grow tandem cells on porous Si substrates.

Coming back to the lack of response in the SiGe bottom cell, it should be noted that the situation here resembles that of a GaInP/Ga(In)As/Ge triple junction solar cell (3JSC) where the EQE of the germanium bottom cell is frequently unmeasurable for a number of reasons (Meusel et al. 2003, Barrigón et al. 2015a). The emitter of our SiGe cell is formed during the growth of the GaInP nucleation layer –as in Ge subcells in 3JSCs– by the concurrent in-diffusion of P, but also of Ga and In, and out-diffusion of Ge from the capping layer. Such a strong atom exchange at the III-V/IV heterointerface, in a material with a high TDD, may produce a p-n junction exhibiting both a low shunt resistance and a low breakdown voltage, which are typical causes for an unmeasurable bottom cell (Barrigón et al. 2015b).

I-V curves under one-sun illumination (AM1.5d ASTM G173 spectrum) of the GaAsP/SiGe tandem cells are presented in Fig. 7.top for the design on porous silicon (red and pink curves) and standard silicon wafers (blue). Again, the red line represents the best device, whilst the thin pink lines are the I-V curves of other cells in the same wafer and thus give an idea of device-to-device variability. The short-circuit current density (J_{SC} = 8.9 mA/cm^2) is in agreement with the integral of the top cell EQE (Fig 5.b). However, as a result of its deliberate limited thickness, we would expect the thin SiGe cell to limit the J_{SC} of the tandem. The absence of this limitation together with the fact that we could not measure the EQE of the SiGe subcell underpin the hypothesis that this subcell is severely shunted, and such level of shunting is quite uniform across the devices manufactured and wafers processed. The magnitude of the J_{SC} measured is obviously low, which is a result of the collection problems discussed around the EQE curves and also of the lack of an ARC. Looking at the shape of the curve around V_{OC}, the impact of a parasitic diode in reverse bias is also evident, which we address below. Apart from this parasitic diode the most remarkable features in the I-V curves are the limited FF and low V_{OC} in both designs. In the case of tandem cells grown on conventional Si substrates, the low shunt resistance is very evident in the I-V curve, causing deleterious effects in both FF and V_{OC}. In (Caño et al. 2020) it was argued that

the shunting was caused by a high crack density in the cell, which behave both as efficient recombination centers for minority carriers and as electrical shorts. However, in the samples grown on porous Si substrates, clear improvements in both FF (from 26.5% to 48.6%) and V_{OC} are observed (from 0.48 to 0.67 V), as a result of lower crack densities. Values are still low but the improvement is evident. In Fig. 7 (bottom) the dark I-V curves of the GaAsP/SiGe tandems are plotted following the same color code as in Fig. 7 (top). The shunt resistances can be visually compared between both structures, being higher in the porous silicon design.

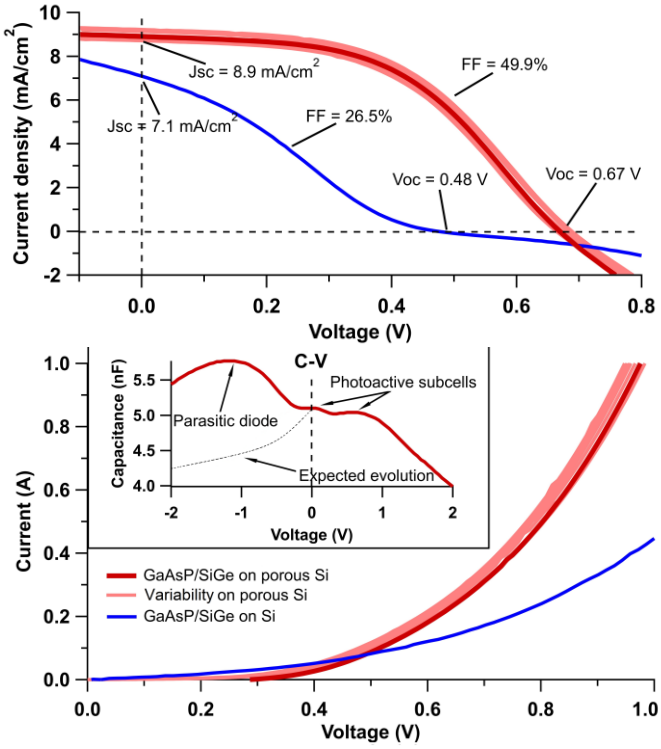

FIGURE 7. (Top panel) Lighted I-V curve of the best GaAsP/SiGe tandem cell grown on porous silicon (thick red line); the thin pink lines represent the I-V curves of most of the devices measured and give an idea of the device-to-device variability; as reference, the illuminated I-V curve of the best GaAsP/SiGe tandem cell grown on standard silicon substrates has been included (blue line) (Caño et al. 2020). (Bottom panel) Dark I-V curves of the solar cells following the same color coding. Inset: C-V curve of a representative device obtained at 300 K under dark conditions. Labels indicate the signature of the different p-n junctions. The thin dashed line qualitatively shows the expected trend without a parasitic diode.

Porous silicon has been reported to have a low electrical conductivity (Zheng et al. 1992, Smestad et al. 1992, Tsai et al. 1993, Jiménez-Cruz et al. 2018), so its impact on

series resistance is a possible concern. However, the presence of the parasitic junction complicates the assessment of the series resistance from the J-Vs in Fig. 7.

In order to confirm the presence of a parasitic diode, C-V measurements were performed on the samples (Fig. 7, bottom inset). The detailed understanding of C-V curves in multijunction solar cells is not straightforward, since only the voltage across the device terminals is known and no information is available about the particular bias at each subcell (Ruiz et al. 2010, Rutzinger et al. 2017, Hoheisel et al. 2011). However, in this case we simply intend to detect the signature of a parasitic diode in reverse bias. The inverse of the total capacitance of the multijunction solar cell (C_T) equals the sum of the inverse of the capacitance of each junction in the device (C_i):

$$\frac{1}{C_T} = \sum_i \frac{1}{C_i} \qquad (1)$$

In principle, in well-behaved cells, it is reasonable to assume that neither the metal/semiconductor contacts nor the tunnel junctions contribute to C_T. In particular, tunnel junctions, being nominally ultra-highly doped, should have a very high junction capacitance and therefore should play a negligible effect in the sum of inverses, which is dominated by the smallest contributions (Ruiz et al. 2010). So in Eq. (1) only capacitance contributions from p/n junctions should be present. As reported by Ruiz et al. in (Ruiz et al. 2010), the C-V curve of a dual junction solar cell with a good tunnel junction would show two humps in the first quadrant –one for each subcell–, a roll-off at high positive voltages, whereas at low positive voltages and under reverse bias the capacitance should steadily decline to its lowest value. We performed C-V measurements at 300K under dark conditions and obtained the curve in the inset of Fig. 7 (bottom). In the positive voltage range, we find the two humps expected followed by the fall of capacitance at high voltages (V>1.3V). These two peaks correspond to the GaAsP and SiGe junctions and, in the second quadrant, we would expect to observe a decline in the capacitance associated with the extension of their space charge regions at negative bias (Ruiz et al 2010). Instead, we find a third peak that we interpret as a third junction in reverse polarity since it shows the expected behavior for the first quadrant but in the second, namely, a fall in capacitance at high voltages, then a peak and finally a decline as we approach 0 volts. This is the signature of a p/n junction in reverse bias,

namely, a parasitic junction, as anticipated from the lighted I-V curves in Fig. 7 (top). We hypothesize that this diode is probably related to the tunnel junction or an adjacent layer. In conventional multijunction cells on Ge substrates, it has been reported that Ge can diffuse over 300 nm into the GaInP nucleation layer, producing strong n-type background doping (Barrutia et al. 2017). In our structure, we have an analogous situation in which a 100 nm n-type GaInP nucleation layer is grown on a Ge cap layer (see Fig. 1). It is possible that Ge diffusion during the growth of the GaAsP top cell may reach the tunnel junction p-side –or its cladding layer–partially compensating its nominally high doping, thereby losing the tunneling properties. This would produce a diode in reverse polarity affecting both the series resistance and the fill factor. The growth of a thicker GaInP nucleation layer could avoid this issue in the future.

In order to get rid of the influence of the parasitic diode and assess the performance limits of the device, we measured the I-V curve at different irradiances and performed a J_{SC}-V_{OC} analysis as shown in Fig 8.a. The J_{SC}-V_{OC} line follows a clear logarithmic trend corresponding to an ideality factor of n=3.6 and a reverse saturation current density of $J_0 = 8.5 \cdot 10^{-3}$ A/cm^2. An ideality factor of 3.6 is in agreement with a device being limited by recombination either in the space charge region or at the junction perimeter, or most likely a combination of both. A high perimeter recombination may be linked to exposed facets in cracks. A high recombination rate within the space charge region is also consistent with the abundance of defects and with the simulations of the EQE, where limited collection in this region had to be assumed. The reconstructed I-V from J_{SC}-V_{OC} measurements is shown in Fig. 8.b together with the experimental I-V. The FF of the reconstructed curve is 63.2%, much better than the real I-V, though still far from the ~80% reported for GaAsP top cells in the best results from the literature (Fan et al. 2019, Grassman et al. 2016). This indicates that, even leaving aside resistive and parasitic diode effects, recombination losses still impact severely the performance of the solar cells. This is another argument for the improvement in the crystallographic quality of the GaAsP top cell as an imperative. In this regard, the GaAsP material quality may be compromised due to the fact that it was grown by MBE. There is evidence that III-V nucleation on Ge –note that the III-V growth takes place on the thin Ge cap (see Fig. 1)– is much more challenging when using MBE vs MOVPE (Li et al. 2001). We are

confident that improvements in GaAsP material quality and top cell performance will be demonstrated using III-V material grown by MOVPE.

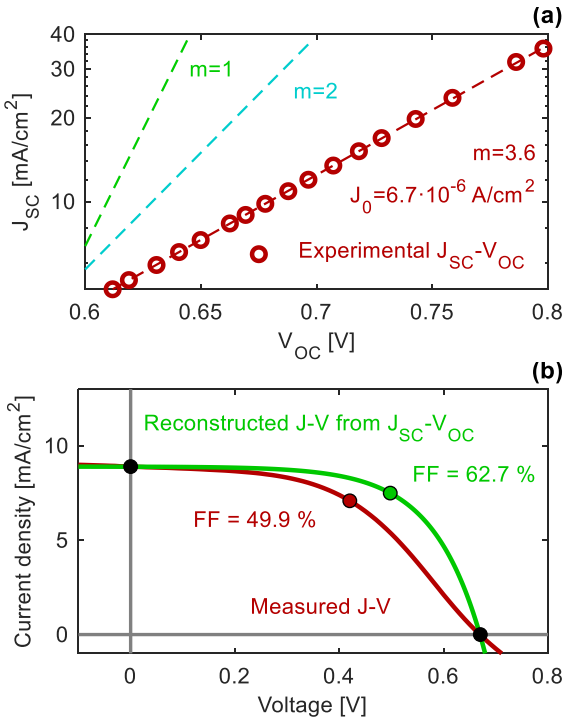

FIGURE 8. (a) JSC–VOC curve of a GaAsP/SiGe tandem cell grown on a porous Si substrate and subsequent fit. (b) Reconstructed illuminated J-V from the JSC-VOC data and measured lighted curve.

The above J_{SC}-V_{OC} analysis is not a direct proof of a working bottom cell. To verify the existence of a working SiGe bottom cell, spectral photovoltage (SPV) measurements were made. The advantage of SPV over EQE is its higher signal to noise ratio and its immunity to series resistance effects. Fig. 9.a shows the SPV response of the GaAsP top cell (in yellow) and SiGe bottom cell (in red). The upsurge in the signal occurs at the bandgap energy in each case (i.e. the energy above which the device is capable of generating voltage), whereas the drop-off is associated with the low-pass filter used in each case. The smoother photovoltage increase observed in the bottom subcell is in agreement with the indirect nature of the SiGe bandgap. On the other hand, the GaAsP top cell shows a sharper edge, related to the expected direct bandgap associated with the P-content, about 20% in this alloy. Fig. 9.b and 9.c depict the fits to obtain the bandgap

energies for the GaAsP top cell and SiGe bottom cell, respectively. These graphs can be interpreted as formally equivalent to Tauc plots in the wavelength range covered. In the case of the GaAsP (Fig. 9.b), as a direct bandgap material, the SPV signal squared at energies close to the bandgap has been assumed to be proportional to the bandgap energy. In the case of the SiGe (Fig. 9.c), as an indirect bandgap material, it is the square root of SPV, which is proportional to E_g for energies near the bandgap energy. The values obtained from the fits agree well with the target design values as well as with the fit obtained from the EQE of the top cell.

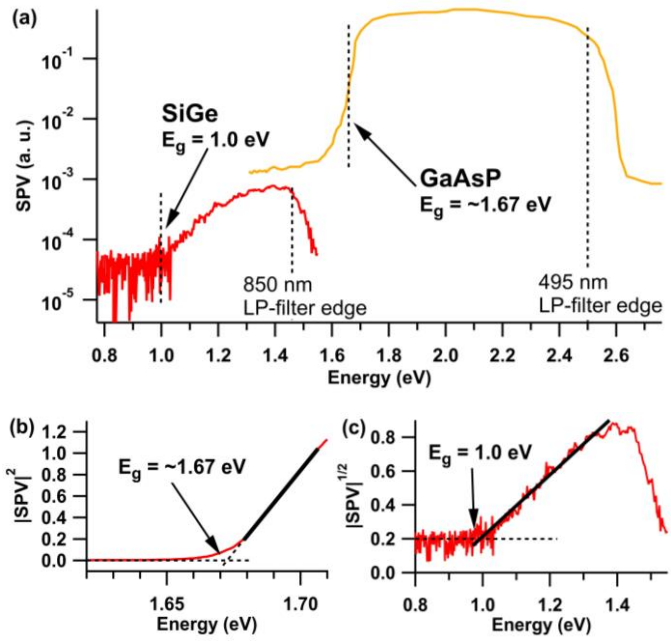

FIGURE 9. (a) Spectral photovoltage measurements of the GaAsP/SiGe tandem cells grown on porous substrates. The red curve corresponds to the bottom cell responses whereas the yellow curve is that of the GaAsP top cell. (b) Fit for obtaining the GaAsP top cell bandgap energy. (c) Fit for obtaining the SiGe bottom cell bandgap energy.

As a concluding point for this study, the responses in the SPV signal of Fig. 9 demonstrate that a truly tandem GaAsP/SiGe solar cell has been grown on a Silicon substrate with a Si porous layer using reverse graded buffers. With this new design, clear improvements in device performance over the results obtained with devices grown on standard Si wafers have been presented. Certainly, these results are still far from

demonstrating that porous silicon layers can be used to solve the problems of reverse graded buffers. However, our findings provide a few evidences in this direction and point towards strategies for further gains in performance.

4. Conclusions

The great impulse in the use of SiGe alloys in the silicon microelectronic industry makes them attractive candidates for the development of tandem solar cells on silicon substrates. As a matter of fact, the combination of III-V compounds with $Si_{1-x}Ge_x$ alloys provides a wide palette of materials to reach optimum bandgap combinations for dual, triple and even quadruple-junction solar cells on silicon. Despite having reached efficiencies over 20%, III-V/SiGe tandem solar cells need to be grown on Si using thick buffer layers (>10μm) which are expensive and eventually lead to the formation of cracks, hindering the development of large area devices. In a search to mitigate these two problems –costly thick buffers and cracking– and move forward in the integration III-V compounds on silicon for photovoltaic applications, GaAsP/SiGe tandem solar cells have been grown on porous silicon substrates through group IV reverse graded buffer layers. Reverse buffers show promise to reduce the threading dislocation density and allow the growth of thinner buffers, although they have been shown to be also prone to cracking. To mitigate this problem, in this study we have used a porous silicon layer incorporated in the substrate to increase its flexibility. In comparison with similar solar cell structures grown on standard substrates, the porous silicon layer has (i) decreased though not eliminated the number of visible cracks, (ii) increased shunt resistance of the structure, (iii) improved the top cell spectral response and (iv) improved the V_{OC} and FF of the cells. However, the overall performance of this design still remains below similar architectures grown on forward graded buffers or on GaP/Si templates. From the results presented it cannot be unequivocally concluded that porous layers solve the problems of reverse graded buffer layers. However, we have presented evidence of partial improvements and proposed a pathway for further gains. We are confident that improvements in GaAsP material quality and cell performance will be demonstrated using III-V material grown by MOVPE.

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