Preliminary Study of Electronics Reliability in ITER Neutron Environment

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Abstract —We validated a method for predicting the Soft Error Rate (SER) in the WEST tokamak operated with deuterium plasmas, and we applied it to predict the SER in the ITER tokamak operated with deuterium-tritium plasmas.

Keywords—CMOS, deuterium–deuterium (D-D), deuterium–tritium (D-T), fusion, neutron, real-time experiment, single event effects (SEE), single-event upset, static random access memory (SRAM), tokamak, ITER, WEST.

Preliminary study of electronics reliability in ITER neutron environment

I. Introduction

The International Thermonuclear Experimental Reactor (ITER) [1] under construction by 35 nations in southern France is a magnetic fusion device that has been designed to prove the feasibility of nuclear fusion as a large-scale and carbon-free source of energy. ITER will use hydrogen isotopes deuterium and tritium to fuel the fusion reaction. From 2035 onwards, at the beginning of the Fusion Plasma Operation (FPO) phase, ITER will be operated with deuterium plasma producing 2.45 MeV neutrons from deuterium–deuterium (D–D) nuclear fusion reactions. Then it will be operated with deuterium–tritium plasma producing, in addition to 2.45 MeV neutrons, 14.1 MeV neutrons from deuterium–tritium (D–T) nuclear fusion reactions. ITER will contain a large amount of electronics for machine command control and diagnosis, which could be exposed to nuclear radiation and negatively affected by this environment. To prevent such a situation, most electronics will be installed in radiation-protected areas (RPAs), and only a limited amount of electronics will be exposed to radiation near the reaction chamber. This work presents the preliminary results of a study currently in progress in ITER, aiming to evaluate the sensitivity of electronic components to the neutron environment of ITER RPAs and determining appropriate countermeasures. The scope of this work is limited to the *soft errors* induced in SRAM memories by neutrons from D–D or D–T nuclear reactions. Other neutron-induced SEE mechanisms, such as latch-up in CMOS circuits and gate rupture or burnout in power devices, will be dealt with in a subsequent study.

II. SER Prediction Method

A. SER prediction model

In the radiation environment of a tokamak operated with D–D or D–T plasma, bit-flips in memory semiconductor devices are caused by secondary particles resulting from interactions of individual neutrons with nuclei of the memory device. The main mechanisms of interaction of neutrons with nuclei are scattering (elastic or inelastic) and absorption (electro-magnetic, charged, neutral and fission).

The Soft Error Rate (SER) per memory bit (bit-flip SER), related to the production of a bit-flip by a secondary particle produced by an incident neutron of energy E interacting with a nucleus is governed by the effective cross-section $\sigma^{SEE}(E)$ of production of the bit-flip by the neutron as a function of its energy E, and by the differential neutron flux as a function of the neutron energy, $d\phi(E)/dE$ (equation 1):

$$SER = \int \sigma^{SEE}(E) \times \frac{d\phi(E)}{dE} dE \qquad (1)$$

In the neutron energy range of a tokamak plasma (thermal to fast neutrons up to 14.1 MeV for D–T plasma, or up to 2.45 MeV plus a small amount of 14.1 MeV for D–D plasma [2]), the effective cross-section $\sigma^{SEE}(E)$ resulting from the various interaction mechanisms can be represented by the following two models:

- The Weibull model representing the interaction of fast neutrons (FN) with nuclei (e.g. silicon), given by:

$$\sigma_{FN}^{SEE}(E) = \sigma_{sat}^{SEE}.\left(1 - e^{-\left(\frac{E-E_{th}}{w}\right)^{s}}\right) \qquad (2)$$

  In this equation (2), the variable E is the neutron energy, and the model's parameters are σ_{sat}^{SEE} (saturation value of $\sigma_{FN}^{SEE}(E)$), E_{th} (threshold energy below which $\sigma_{FN}^{SEE}(E) = 0$), w (scale parameter) and s (shape parameter).

- The thermal neutron interaction model representing the interaction of thermal neutrons (ThN) with ^{10}B nuclei ($^{10}B(n,\alpha)^{7}Li$), given by:

$$\sigma_{ThN}^{SEE}(E) = \sigma_{E_{Th}}^{SEE}.\sqrt{\frac{E_{Th}}{E}} \qquad (3)$$

  In this equation, $\sigma_{E_{Th}}^{SEE}$ is the cross section of SEE production in the considered memory by ionized secondary particles resulting from the interaction with ^{10}B of neutrons having an energy E_{Th}=25 meV, and the $\sqrt{E}$ behavior is linked to the neutron absorption probability as a function of energy.

B. Test of the SER prediction model

The SER prediction method based on eq. (1), already successfully used e.g. for the neutron environment of the LHC collider [7], was tested for the neutron environment of a Tokamak using the Real Time Single Event Rate (RTSER) test bench [2], [3], [4] developed by IM2NP (Institut Matériaux Microélectronique Nanosciences de Provence, Aix-Marseille University) and STMicroelectronics to study the mechanisms of production of SEEs by atmospheric neutrons on semiconductor memories. This RTSER test bench embeds 384 memory circuits (3,226 Gbit in total) manufactured by STMicroelectronics in CMOS 65 nm bulk technology with fabrication processes based on a BPSG (Borophosphosilicate Glass)-free BEOL that eliminates the major source of ^{10}B in the circuits and drastically reduces the possible interaction between ^{10}B and very low (thermal) energy neutrons. The four parameters of the Weibull model (2) of RTSER ($\sigma_{sat}^{SEE} = 3.17 \times 10^{-15}\,cm^2/bit$, $E_{th} = 0.148\,MeV$, $w = 9.11\,MeV$ and $s = 0.856$) were determined using an optimization algorithm to best fit to the experimental values of $(E\sigma_{FN}^{SEE}(E), E)$ measured on RTSER at neutron energies $E_1 = 13.94\,MeV$, $E_2 = 2.06\,MeV$ and $E_3 = 0.48\,MeV$ in the AMANDE neutron facility of IRSN in Cadarache [2].

The RTSER test bench was operated in the D–D plasma neutron environment of the WEST tokamak [2]. WEST is an experimental nuclear fusion device operated by the IRFM (Institute for Magnetic Fusion Research) institute from CEA (French Alternative Energies and Atomic Energy Commission) in Cadarache, France [5]. Table I summarizes the results from measurements performed on RTSER exposed to D–D plasma neutrons at 3 positions in the WEST torus hall (TH-1, TH-2 and TH-3, all in equatorial plan, respectively at radial position 10.3 m; 6.5 m and 5.2 m from the tokamak magnetic axis) and gives the cumulated values for these three positions (column "All"). The experimental SER, determined from column "All", is equal to $6.18 \times 10^{-3}\ s^{-1}/Gbit$.

TABLE I.

Position	**TH-1**	**TH-2**	**TH-3**	**All**
Number of pulses	32	133	74	239
Cumulated pulses duration (s)	320	909	678	1907
Cumulated neutron fluence (cm^{-2})	7.7E5	1.2E7	1.6E7	2.8E7
Number of bit-flips	0	8	30	38

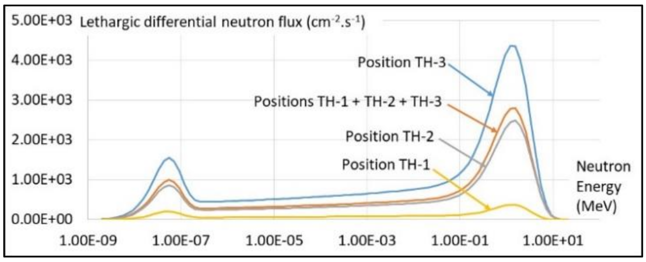

Fig. 1. Differential neutron flux per lethargy at positions TH-1, TH-2 and TH-3

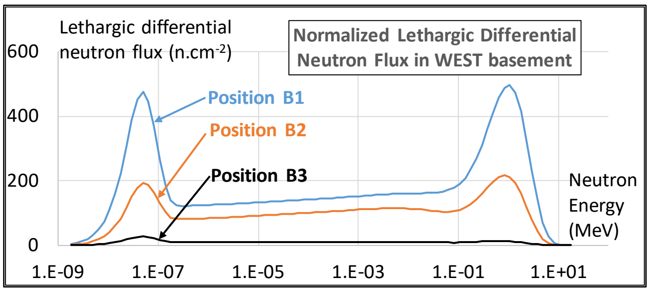

Fig. 2. Differential neutron flux per lethargy at positions B1, B2 and B3

Fig. 1 gives the neutron energy spectrum measured at the location of the RTSER test bench during bit-flip measurement at positions TH-1, TH-2 and TH-3. The fast neutrons peak around 1–2 MeV corresponds to D-D neutrons, initially emitted at 2.45 MeV in the plasma bulk and transported outside the tokamak chamber. The spectrum measurements were performed using a commercial neutron spectrometer called DIAMON (Direction aware Isotropic and Active neutron MONitor) [6]. The orange curve represents a unique spectrum from the contribution of the three measured spectra. It is obtained by dividing the sum of the neutron *fluence* spectrum at the three positions by the total time of exposure at the three positions.

Eq. (1) allows to predict the average SER for positions TH-1 + TH-2 + TH-3, using the Weilbull model's parameters of the RTSER test bench determined at AMANDE and using the above global neutron energy spectrum for positions TH-1 + TH-2 + TH-3. The SER thus calculated is equal to $3.90 \times 10^{-3}\ s^{-1}/Gbit$. The ratio between the predicted and measured SER is equal to 0.63, which is very satisfactory for the purpose of using the SER prediction method in ITER.

This result validates the SER prediction method based on equation (1) for the specific case of a device (the RTSER memory bank) which is expected to have a limited sensitivity to thermal neutrons thanks to the absence of BPSG in its manufacturing process. Other experiments on other devices will be needed to validate the method in the general case of devices sensitive to both fast neutrons and thermal neutrons.

III. Bit-flips in WEST control electronics

The control electronics of WEST systems is located in the basement of the tokamak building, protected from radiations by an 80 cm slab made of heavy borated concrete. During WEST's C2 to C5 D–D plasma campaigns (7.5 hours of D-D plasma in total), WEST systems have undergone about one hundred untimely stops for undetermined causes (approximate estimate, because these stops were not recorded nor analysed). Some of these failures were corrected by rebooting the electronics (including a rewrite of configuration memories): such failures could result from neutron-induced bit-flips in configuration memories. The correction of the other failures required a power cycling (the reboot was not able to correct them): such failures could result from neutron-induced latch-up or SEFI (Single-Event Failure Interrupt) in CMOS circuits.

We present below the application of the method described in chapter II, to the estimate of the number of neutron-induced bit-flips during C2 to C5 campaigns in the WEST electronics.

A. Neutron energy spectrum

Fig. 2 shows the normalized aggregated differential neutron flux per lethargy measured with the DIAMON spectrometer during C5 D–D plasmas at three radial positions, B1 (2.4 m), B2 (6.3 m) and B3 (11.9 m), representative of the location of the control electronics in WEST tokamak building basement. The normalization factor, applied to the spectrum measured during campaign C5, is the ratio between the average neutron production rate during campaigns C2 to C5 and the neutron production rate during campaign C5.

B. Bit-flips evaluation vehicle

The scope of the study was limited to the bit-flips induced by neutrons on the configuration memories present in the electronics installed in the basement of WEST. The amount of configuration memories was estimated to about 1 Gbit. This estimate was made by analyzing the datasheets of each concerned electronic circuit.

To evaluate the sensitivity of WEST's electronics to neutron-induced bit-flips in configuration SRAMs, instead of testing WEST's electronic systems (not practically doable), we adopted as SER evaluation vehicle a preliminary set of SRAM memories from various technological nodes, whose model parameters are published [7]. Table II gives the list of the selected components, as well as their model parameters. In this table, the nodes are in nm, the Weibull parameters σ_{sat}^{SEE} , E_{th} and w are in cm^2/bit, MeV and MeV, and the thermal neutron interaction model σ_{sat}^{SEE} is in cm^2/bit.

Fig. 3 established from Eqs. (1), (2) and (3) gives, for 1 Gbit of the three SRAM memories of Table II, the total number of bit-flips expected under the effect of the neutron flux (ThN + FN) of campaigns C2 to C5 of WEST (7.5 hours of cumulated D–D plasma; normalized neutron energy spectrum given by Fig. 2).

TABLE II. SET OF SRAM MEMORIES

Device	**Node**	σ_{sat}^{SEE}	E_{th}	w	s	σ_{ThN}^{SEE}
IS61WV204816 BLL-10TLI [7]	40	1.40 $\times 10^{-14}$	0.01	14.05	0.82	4.25 $\times 10^{-15}$
CY62157EV30L L-45ZSXI [7]	90	2.16 $\times 10^{-13}$	0.1	24.22	1.98	2.15 $\times 10^{-15}$
AT68166H-YM20-E [7]	250	2.60 $\times 10^{-13}$	0.2	13.08	2.99	3.38 $\times 10^{-15}$

Although the sampling adopted for this preliminary study is very small, the estimated average (58) and maximum (176) numbers of bit-flips are compatible with the ca. one hundred untimely stops observed (but not documented) by IRFM technical staff during campaigns C2 to C5 of WEST. This result confirms the applicability of the method to predict the SER of the electronics of a tokamak in its neutron environment, taking into account both thermal and fast neutrons.

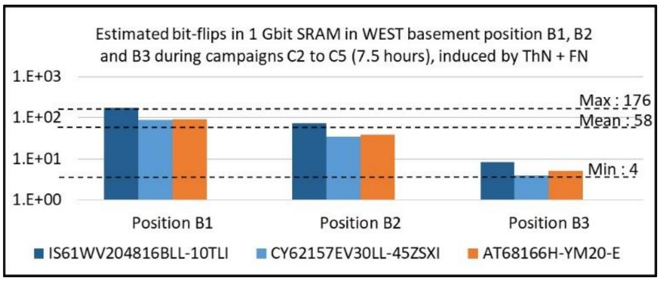

Fig. 3. Bit-flips in selected memories at positions B1, B2 and B3

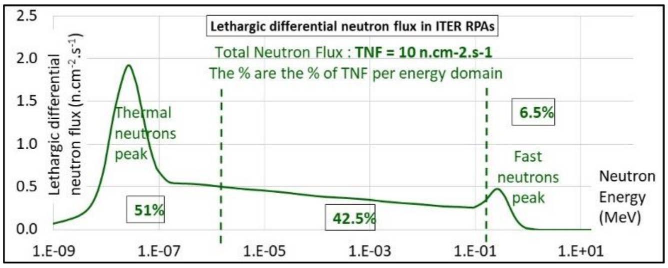

Fig. 4. Differential neutron flux per lethargy in ITER Radiation Protected Areas

IV. Bit-flips in ITER control electronics

A. Background

Most of the ITER control electronics will be installed in in specific places called Radiation Protected Areas (RPA), most of them created in the corners of the tokamak complex building. In these RPAs, for the entire duration of the tokamak operation during the fusion plasma operation (FPO) phase (4700 hours of 500 MW D–T plasma), the radiation environment will not exceed a total ionizing dose (TID) of 1 Gy (Si), an equivalent neutron fluence (ENF) of 10^8 n.cm^{-2} (1 MeV Si eq. n.cm^{-2}) and a total neutron flux (TNF) of 10 n.cm^{-2}.s^{-1} (full energy spectrum). Such levels of TID and ENF are deemed harmless for electronics. In several RPAs, the TNF will approach or reach the upper limit of 10 n.cm^{-2}.s^{-1} and might have an impact on electronics reliability, which shall be corrected by means of appropriate local neutron shielding. The design of these local shields depends on the attenuation factor required for thermal neutrons and for fast neutrons.

B. Electronics considered for this preliminary study

The attenuation factors required for the local shields depend on the reliability and availability requirements applicable to the electronics installed in the RPAs. The ITER Research Plan requires an overall availability of 60%. The actual availability will depend on the rate of failures making the tokamak unavailable, and on the Mean Time To Repair (MTTR). The failures making the tokamak unavailable are mainly those that impact (i) a system necessary for the operation of the tokamak or (ii) a diagnostic necessary for the scientific program of the experiments in progress. The neutron-induced failures on memory circuits, likely to cause that type of unavailability, are mainly bit-flips in the configuration memories of digital circuits such as microprocessors, microcontrollers and FPGAs. These failures require a reboot of the systems concerned. Conversely, bit-flips in data buffers generally do not cause failures because they are effectively filtered out.

Of the configuration memories, SRAMs are the most sensitive to neutron-induced bit-flips. This is why the present preliminary study is focused on configuration SRAMs. A preliminary analysis has allowed to estimate at about 100 Gbits the total amount of configuration SRAM memory used in the electronics installed in the RPAs of ITER tokamak building. This figure is probably an underestimate because a more detailed analysis in progress at the time of this writing shows more than 15 Gbits of configuration SRAM memory in only one of the ITER systems, out of a total of more than 30 systems. Nevertheless, this preliminary estimate of 100 Gbits was adopted for the present preliminary study.

C. Neutron environment in ITER Radiation Protected Areas

Fig. 4 shows the energy spectrum of neutrons in the RPAs of the ITER tokamak building, normalized to the maximum flux of 10 n.cm^{-2}.s^{-1} expected in these RPAs during the Fusion Plasma Operation (FPO) phase. This spectrum was obtained from neutron fluxes per bins of energy, obtained by Monte-Carlo simulation (MCNP), taking into account the neutron sources (plasma, activated water) during operation of the tokamak at full D–T plasma power (500 MW) as well as the structural components of the tokamak complex building.

The thermal neutron peak shown in Fig. 4 is much higher than the fast neutron peak, due to the strong energy degradation induced by the large neutron flux attenuation factor ($\sim 10^8$) provided by the structural components of the building.

D. Bit-flips in configuration SRAMs in RPAs during FPO

As in the case of WEST (chapter III), the reference components retained to represent ITER electronics for this preliminary study of bit-flips in the electronics housed in the RPAs of the ITER tokamak building are those identified in Table II.

Eq. (1) associated with Eqs. (2) and (3) makes it possible, by using the model parameters given in Table II for these three reference components, to estimate the SER of 100 Gbits of configuration SRAMs of the electronics installed in the RPAs of the ITER tokamak building.

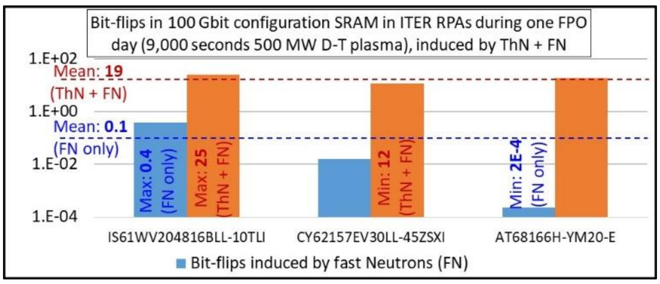

Fig. 5. Bit flips per FPO day in 100 Gbits of the 3 reference SRAMs

The ITER Research Plan foresees about 9,000 seconds of cumulated D–T plasma duration at full power (500 MW), per operation day in the FPO phase. This duration can be made of nineteen plasma pulses of 450 seconds, or nine plasma pulses of 1,000 seconds, or three plasma pulses of 3,000 seconds. This daily plasma duration makes it possible to calculate, from the estimated SER, the number of bit-flips per FPO day of D–T plasma expected in the estimated 100 Gbits of electronic configuration SRAMs installed in the RPAs of the ITER tokamak building. Fig. 5 shows the result of this estimate for the 3 reference SRAM memories of Table II.

E. Implications for ITER electronics availability

If each bit-flip induces a failure requiring reboot/reset of the electronic system concerned (which is a reasonably conservative hypothesis for bit-flips impacting configuration programs), the preliminary estimate given by Fig. 5 is an average number of about 20 failures per day, with a maximum of about 25 and a minimum of about 10.

ITER systems are subject to a rule that imposes the possibility of a remote reboot, which should make it possible to quickly restore normal operation of the system concerned by a failure requiring a reboot. However, with an average of about 20 failures per day, during any FPO operation day based on twenty pulses of 450 seconds or nine pulses of 1,000 seconds or three pulses of 3,000 seconds, all the plasma pulses of the day are likely to be impacted by a failure requiring reboot.

In the case of 3 plasma pulses of 3,000 seconds per day, the 60% availability required by the ITER Research Plan implies being able to achieve two pulses of 3,000 seconds without failure and one pulse of 3,000 seconds possibly with a failure. With an availability based on successfully completed plasma pulses, this requires a failure rate of no more than about 0.3/day.

To secure a failure rate of about 0.3/day, the maximum failure rate (25/day) predicted by this preliminary study should be divided by a factor of about 80. Fig. 5 shows that the failure rate is mostly governed by thermal neutrons. Thanks to the high thermal neutron capture cross section of ^{10}B [8], present at 20% in natural boron, it should be possible to reduce the flux of thermal neutrons by a factor of 100, or even 1000 if necessary, by means of a thin local shielding (a few mm) of B_4C on cabinets housing electronics. Fig. 5 shows that, with this thermal neutron shielding, the residual failure rate induced by fast neutrons only would be at most about 0.4 / day, which is close to the upper limit of about 0.3 failure / day needed to secure the 60% reliability requested by the ITER Research Plan.

V. CONCLUSION AND NEXT STEPS

We developed a method that allows to predict with a good accuracy the failure rate on electronics, induced by neutrons with a given flux and energy spectrum in a tokamak. This method has been successfully validated by comparing the error rate predicted and measured on an electronic test bench exposed to D–D neutrons in WEST tokamak. Predictions and measurements differ by about 30% only, which is very satisfactory for the purpose of predicting failure rates on electronics in ITER.

This method made it possible to show that the ca. one hundred of untimely stops observed by the IRFM on WEST tokamak systems during the C2 to C5 experimental campaigns of WEST can be explained by bit-flips induced by neutrons in the configuration SRAM memories of the electronic circuits installed in the basement of WEST tokamak building.

This method was then applied to perform a preliminary study of the reliability of electronics in ITER, using published data of models of cross section of bit-flip production by neutrons in semiconductor SRAM memories. This preliminary study shows that in ITER Radiation Protected Areas, the neutron flux could cause on average about 20 failures per day, requiring a restart of the concerned system. To comply with the planned scenario of plasma pulse duration in fusion plasma operation and with the targeted availability of 60% adopted by the ITER Research Plan, in RPAs, thanks to the fact that the neutron-induced failure rate is mostly driven by thermal neutrons, the *thermal neutron flux only* needs to be attenuated, by a factor of about 80 which can be achieved with a thin (few mm) boron carbide local shielding on cabinets housing electronics. No shielding other than this thin layer will be needed at the building level and there will be no impact on the reference configuration.

The figures given by this study are preliminary, because they are based on a limited sampling of electronic devices which does not represent the diversity of modern electronics in general, and they does not take into account SEE mechanisms other than neutron-induced bit-flips, such as latch-up in digital electronics and burnout or gate rupture in power devices present in all electronic systems (which are however less likely to be induced by neutrons below 20 MeV when compared to soft errors).

A detailed study of the reliability of electronics in ITER should follow, to consolidate the present preliminary results in order to provide inputs needed for the design of local shields to be installed on electronic cabinets in RPAs. This detailed study should be conducted at device level, with a broader sampling of devices, technology nodes and manufacturers and should take into account various SEE mechanisms such as bit-flips, latch-up, burnout and gate rupture.

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