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# Fusion Neutron-Induced Soft Errors During Long Pulse D-D Plasma Discharges in the WEST Tokamak

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*Abstract* — We conducted real-time SER measurements on bulk 65 nm SRAMs in the WEST tokamak during long pulse deuterium-deuterium plasma discharges (~60 s), evidencing bursts of SEUs during the most efficient shots and 12% of MCU events.

**Keywords**—CMOS, deuterium–deuterium (D-D), deuterium–tritium (D-T), fusion, neutron, real-time experiment, single event effects (SEE), single-event upset, static random access memory (SRAM), tokamak, ITER, WEST.

# Fusion Neutron-Induced Soft Errors During Long Pulse D-D Plasma Discharges in the WEST Tokamak

## I. INTRODUCTION

THE WEST tokamak [1] is a research device operated by CEA-IRFM and designed to develop the technology necessary for fusion power [2]. WEST serves as a complementary research tool to the International Thermonuclear Experimental Reactor, the ITER project [3], with a focus on testing new materials, exploring new plasma confinement regimes, and developing steady-state operation [4]. While WEST uses deuterium–deuterium (D-D) plasma and ITER will work with deuterium–tritium (D-T) plasma, the research conducted at the WEST tokamak can still provide valuable insights into the behavior of high-temperature plasmas and the development of new materials and technologies for future fusion reactors. D-D reactions will therefore be used during ITER development and commissioning before introducing tritium fuel. Because both D-D and D-T operations produce a high flux of energetic neutrons, creating a residual neutron field outside the reaction chamber [5], the electronics for command control and diagnosis of all future fusion devices will be exposed to nuclear radiation and negatively affected by this environment. Investigations are necessary to quantify such radiation effects on electronics devices, circuits and systems in the perspective of qualification procedures and guidelines [6].

In 2020-2021, we conducted the very first real-time soft-error rate characterization of CMOS bulk 65-nm static random-access memories (SRAMs) subjected to fusion neutrons during D-D plasma operation at WEST (C5 campaign) [7]. The test equipment, installed in the experimental hall in the proximity of the tokamak, was irradiated during machine shots ranging from 1 to 18 s in duration. A total of 48 bit flips were detected for a cumulated neutron fluence of  $1.43 \times 10^8$  n.cm<sup>-2</sup> at device level obtained after 1,252 s (0.348 h) of machine operation [7].

This year, new real-time SER measurements with the same setup were performed during the WEST C7 experimental campaign. This latter was characterized by a series of very long pulse (up to 109 s) and very efficient D-D plasma discharges (up to  $10^{14}$  neutrons per shot). The present work summarizes the new experimental results obtained under these conditions, characterized by an improved SEU event statistics, with more than 5 times more bit flips than during C5 campaign. Results presented in the following also demonstrate the reproducibility of the measurements and evidence the occurrence of bursts of SEUs during the most efficient machine shots. The comparison

of this new data with numerical simulation is finally reported and discussed.

## II. EXPERIMENTAL DETAILS

The real-time SER test setup used for the C5 campaign (see details in [7]) has been reused in the same experimental conditions for the present work at a distance of 5.2 m from the center of the tokamak (position P3 in [7], see Fig. 1). We recall here that the setup contains 384 SRAM circuits manufactured in CMOS bulk 65 nm by STMicroelectronics from a boron-10 free manufacturing process. Each test chip contains 8.5 Mbits of single-port SRAM (without deep-N-well) with a bit cell area of  $0.525 \mu\text{m}^2$ , operated under a nominal core voltage of 1.2 V. During measurements, the tester scans the full memory plan ( $384 \times 8.5 \times 1024^2 = 3.422$  Gbit) one time every 2.5 s. The SRAM circuits with their upper face oriented toward the center of the machine were placed in the equatorial plane of the tokamak.

The neutron flux monitoring during the machine shots were obtained from the WEST fission chambers (CAF) positioned around the tokamak. During the C5 campaign, we performed neutron metrology using a commercial DIAMON neutron spectrometer [8] to accurately determine the neutron fluence at the level of the test bench. From CAF data and using a

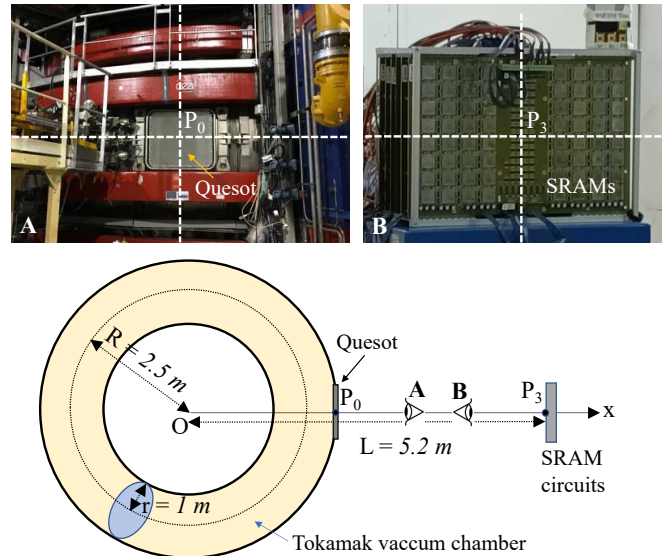


Fig. 1. Schematic top view and photos of the tokamak (A) with the real-time test setup (B) installed at the position P3 in front of the quesot center P0 in the tokamak equatorial plan.

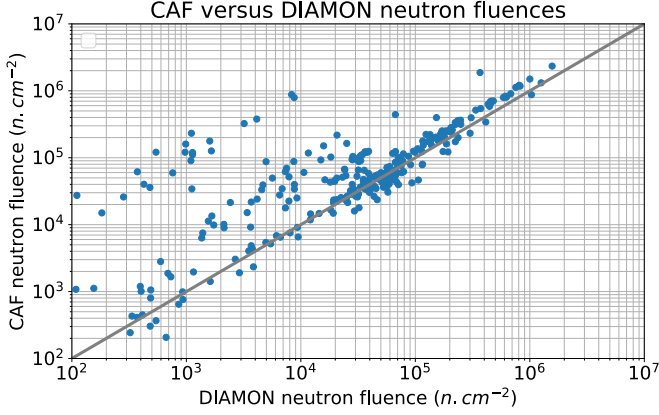


Fig.2. Neutron fluence at the level of the test bench (SRAM circuits) determined from CAF measurements using the numerical model described in [7] versus direct measurements obtained using the DIAMON spectrometer. During C7 campaign, shot neutron fluences are all above  $10^5$  n/cm<sup>2</sup> that corresponds to the domain of the curve where CAF versus DIAMON correlation is excellent.

numerical model described in [7], we were able to predict the neutron fluence at the level of the test bench with a good agreement with respect to fluences measured using the DIAMON spectrometer. Fig. 2 shows the correlation between neutron fluences determined by CAF + numerical model and measured by DIAMON at the level of the exposed circuits. For the C7 campaign, all shot neutron fluences are above  $10^5$  n/cm<sup>2</sup> that corresponds to the domain of the curve where CAF versus DIAMON correlation is excellent.

### III. EXPERIMENTAL RESULTS

The real-time SER test equipment was installed and operated for 5 weeks during the WEST C7 campaign with a full capacity of 3.422 Gbit. A total of 451 machine shots were produced during this period for a cumulated duration of 8,832 s and a cumulated neutron fluence (at the level of the circuits under test) of  $1.03 \times 10^9$  n.cm<sup>-2</sup>. 168 shots were identified to have induced SEUs.

Figs. 3 (a) and (b) show the distribution of the number of neutrons produced during shots and the distribution of shot durations for all the events, respectively. Machine shots during which SEU events have been detected in coincidence with the neutron flux are indicated in red. Fig. 4 combines data of Figs. 3 (a) and (b) to show the number of neutrons produced per shot versus shot durations. On one hand, 110 on the 121 shots (91%) having produced more than  $10^{13}$  neutrons induced SEU(s). On the other hand, only 5 pulses on the 279 (1.8%) having produced less than  $10^{12}$  neutrons induced SEU(s). There is clearly a threshold effect between  $10^{12}$  and  $10^{13}$  neutrons/shot for the production of SEUs.

Concerning the SBU, MCU and bit flips distributions, a total of 189 SBUs, 14 MCU(2), 11 MCU(3) and 1 MCU(10) have been detected in coincidence with machine shots, representing a total of 260 bit flips. Two additional events (1 SBU and 1 MCU(2)) have been detected during machine shutdown, that roughly corresponds to the SER of the test bench in the natural radiation background [9].

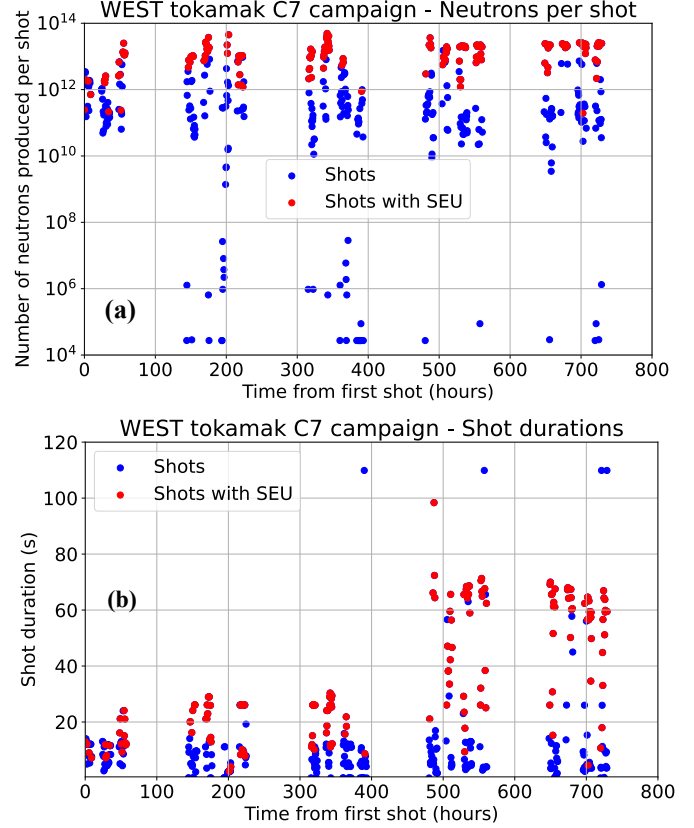


Fig. 3. Distribution of the number of neutrons produced during machine shots and distribution of shot durations for all the shots of the WEST C7 campaign (5 weeks). Machine shots during which SEU events have been detected in coincidence with the neutron flux are indicated in red.

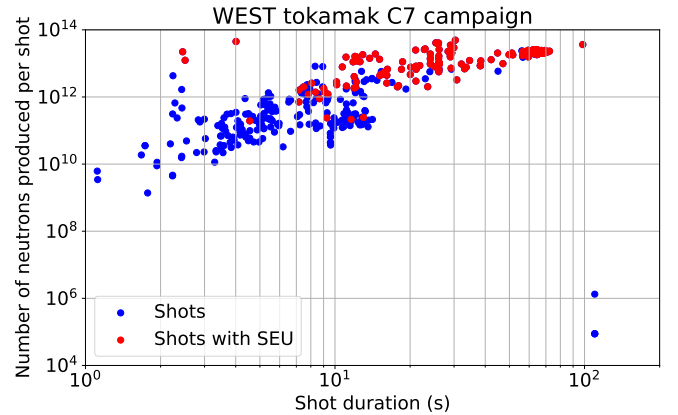


Fig. 4. Distribution of the number of neutrons produced during machine shots versus shot duration for all the shots of the WEST C7 campaign. Machine shots during which SEU events have been detected in coincidence with the neutron flux are indicated in red.

Fig. 5 shows the bit flip distribution as a function of the cumulated neutron fluence evaluated at the level of the circuits for all the events detected during the WEST C7 campaign. By comparison, we plotted the 48 bit flips detected during the C5 campaign for a cumulated neutron fluence of  $1.43 \times 10^8$  n.cm<sup>-2</sup> reached at the end of the campaign. The bit flip statistics has been improved by a factor  $\times 5$  in C7 with respect to C5.

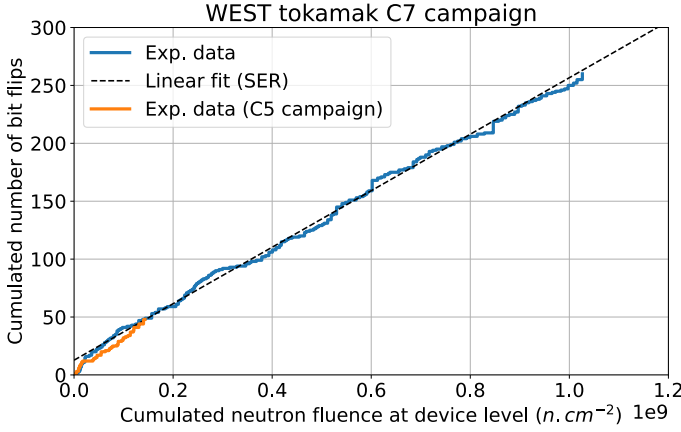


Fig. 5. Bit flip distribution as a function of neutron fluence for all the events detected during the WEST C7 and C5 campaigns. The linear fit corresponds to the extraction of the bit flip SER for data related to C7.

TABLE I  
SUMMARY OF C5 AND C7 CAMPAIGN IN TERMS OF SEUs

	C7 campaign (2023)	C5 campaign (2021)
Maximum shot durations (s)	109	18
Maximum neutrons/shot (tokamak)	$5 \times 10^{13}$	$1 \times 10^{13}$
Cumulated neutron fluence ( $n.cm^{-2}$ ) at device level	$1.03 \times 10^9$	$1.43 \times 10^8$
Single Bit Upsets (SBU)	189 (87.9%)	36 (87.8%)
MCU events	26 (12.1%)	5 (12.2%)
MCU(2)	14	3
MCU(3)	11	2
MCU(>3)	1 MCU(10)	0
Total SBU + MCU events	215	41
Total bit-flips	260	48

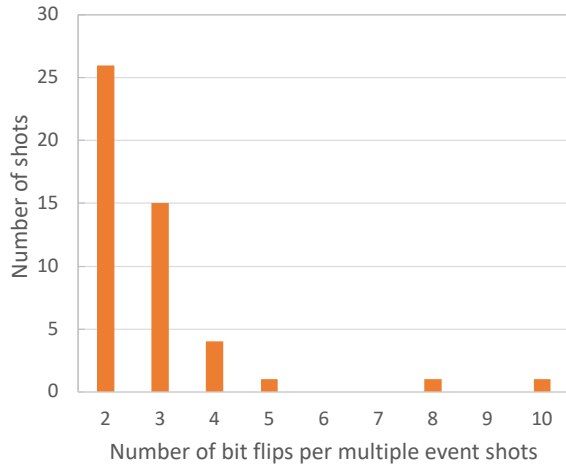


Fig. 6. Histogram of multiple events shots as a function of the number of bit flips detected during the same shot. A 2 bit flip occurrence can correspond to 2 SBUs or 1 MCU(2), a triple bit flip occurrence to 3 SBUs, 1 SBU and 1 MCU(2) or 1 MCU(3), etc.

Such a higher statistics can explain the detection of a rare MCU event with a multiplicity of 10 (with all adjacent cells in the physical plan of the memory circuit).

Table I compares results obtained during the two campaigns in terms of SBU and MCU ratio. SBUs (resp. MCUs) represent 88% (resp. 12%) of the detected events, these ratios are identical for the two campaigns, that demonstrates a good repeatability of both irradiation conditions and measurements.

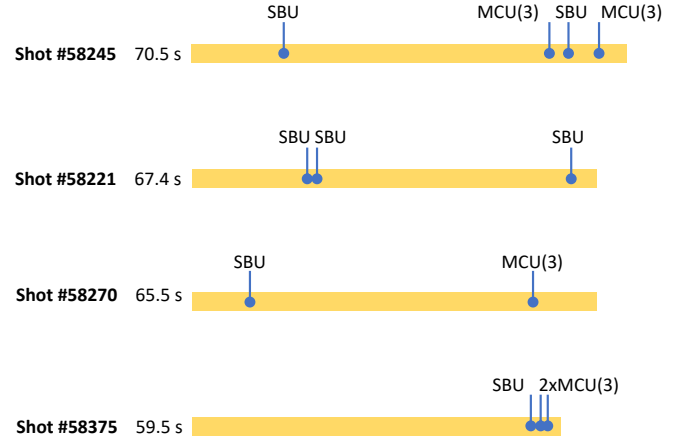


Fig. 7. Time distribution of SEUs during a few long shots characterized by the occurrence of multiple events.

With respect to a reference neutron flux of  $20 n \cdot cm^{-2} h^{-1}$ , the tokamak radiation environment gives an acceleration factor of real-time experiment equal to  $AF = 2.09 \times 10^7$ . The corresponding bit flip SER under tokamak radiation is equal to  $n-SER = 3.3 \times 10^7$  FIT/Mbit and the bit flip neutron cross section for SRAM in the tokamak field is  $\sigma_n = 7.1 \times 10^{-17} cm^2/bit$ .

Another important and new result obtained in the present work concerns the occurrence of multiple SEU events, that we called “burst events” during the same machine shots. On 168 shots having produced SEUs, 48 shots (between the most efficient in terms of neutron production) resulted in multiple SEU events, i.e., 2 or more SBUs, MCUs or a combination of SBUs and MCUs detected in coincidence with a given shot. Fig. 6 shows the histograms characterizing these burst events in terms of number of bit flips. Double SBU events have been detected during 21 machine shots, triple SBUs 3 times and quadruple SBU 1 time.

Due to the short reading/verification cycle of our test bench (as we mentioned, the full memory plan is scanned one time every 2.5 s), the occurrence of multiple events can be resolved in time during a machine shot if the clock of the tester is synchronized with the clock of the tokamak facility. Fig. 7 shows the time distribution of SEUs during a few long shots characterized by the occurrence of 2, 3 and 4 events. One can notice that MCU events are systematically observed in the last part of these long pulses whereas SBUs are more uniformly distributed throughout the whole duration of the pulse.

#### IV. DISCUSSION

These new experimental results obtained during the WEST C7 campaign confirm and bring new elements about the possible role of triton burn-up neutrons in the production of SEUs, a mechanism invoked in [7] to explain the occurrence of MCU events in previous experiments. For memory, once D-D fusion is correctly initiated at the beginning of a machine shot, the concentration of 1 MeV tritons (produced in one of the two D-D reactions) gradually increases in the plasma and renders possible D-T fusion. This process is known as “triton burn-up” and 14-MeV neutrons produced in D-T reactions occurring in deuterium discharges are called “triton burn-up neutrons” (TBNs) [10]. Only such “high energy” neutrons, with respect to



primary 2.45 MeV neutrons produced in D-D reactions, can explain the production (during nonelastic reactions) of secondary fragments with sufficient long ranges in silicon, a necessary condition to observe MCU events in the considered 65 nm SRAM circuit [7]. In the current work, 26 MCUs events have been detected for a total neutron fluence of  $1.03 \times 10^9$  n.cm<sup>-2</sup> at device level. Considering that we previously observed 37 MCUs for  $4.17 \times 10^7$  n.cm<sup>-2</sup> of pure 14 MeV neutrons at AMANDE (IRSN) facility [11] with the same setup loaded at 3.224 Gbit [7], the combination of these different results shows that “high energy” D-T neutrons should represent 2.7% of the total D-D + D-T neutron fluence estimated at circuit level.

Fig. 8 shows bit flip distributions obtained by numerical simulation [12] for different D-T/D-D neutron fluence ratios ranging from 0% to 5%. Without the contributions of D-T neutrons, there is an evident deficit of bit flips for a cumulated neutron fluence corresponding to that estimated at circuit level for the C7 campaign ( $1.03 \times 10^9$  n.cm<sup>-2</sup>). Increasing the fraction of D-T neutrons causes MCU events to occur. Experimental data is well fitted with the bit flip distribution simulated with a ratio precisely equal to 2.7%, confirming the raw extraction from MCU statistics.

This percentage is in good agreement with triton burnup ratio reported in several studies, typically between 1 and 3% [10, 13, 14]. As explained in [14], the production of 14 MeV neutrons depends on the conditions of 1.01 MeV triton confinement and thermalization. Such a process is easy to achieve in pulses with higher plasma current in order to reduce triton Larmor radius: there is a correlation between measured the D-T/D-D ratio and the plasma current or electron temperature.

Another experimental observation supporting the role of D-T neutrons in the production of MCUs is the occurrence of these events in the last part of pulses, as clearly shown in Fig. 7. This result is in very good agreement with the fact that the triton concentration in the plasma increases from the beginning to the end of a shot [10] (the triton burn-up neutron emission also goes with some delay relative to the birth time of triton). During a pulse, the plasma is gradually enriched in tritium, which promotes the production of 14 MeV neutrons, and therefore the probability of production of MCUs is maximum when the tritium concentration is maximum, i.e. at the end of the plasma pulse.

Although the measurements were performed on another tokamak under possibly different operating conditions, Fig. 2 in [13] shows time-resolved profiles of D-D, D-T and D-T/D-D ratios during a D-D discharge at the JET tokamak. The D-T/D-D ratio exhibit a peak at the end of the machine shot, reaching 1.5% for a low plasma current (1.5 MA). Fig. 3 in the same reference shows that increasing the plasma current to 6 MA leads to a D-T/D-D ratio larger than 3%.

Qualitatively speaking, similar time evolution and magnitude of this D-T/D-D ratio in the WEST tokamak should perfectly explain the occurrences as well as the time distributions of the observed MCUs in the present experiment. Machine shot parameters delivered by the WEST control command and time-domain analysis of MCUs related to all events will be systematically investigated and tentatively correlated in the final work. New quantitative projections for ITER operation will be also estimated from these new results.

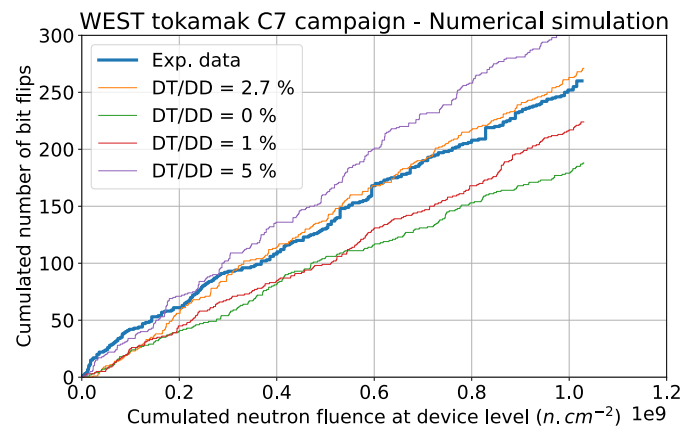


Fig. 8. Comparison between experimental and simulated bit flip distributions for the C7 campaign. Numerical curves have been obtained for different values of the D-T/D-D ratio: 0%, 1%, 2.7% and 5%.

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