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Impact of Total Ionizing Dose on the alpha-Soft Error Rate in FDSOI 28 nm SRAMs

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Abstract – Synergy effect of total ionizing dose (TID) on alpha-soft error rate (α -SER) in FDSOI 28nm SRAM has been experimentally characterized using a dedicated setup combining alpha-particle irradiation (²⁴¹Am solid source) in vacuum chamber and 10 keV X-ray irradiation. Measurements have been performed on a 3 Mbit single-port SRAM cut powered at 1V. Irradiations up to 125 krad(Si) have been achieved and their impact on the α -SER has been characterized from the cumulated number of bitflips as a function of the exposition time to the alpha-source. Modelling and simulation have been used to link transistor threshold voltage variations to SRAM cell stability in terms of static noise margin (SNM), critical charge (Q_{crit}) and finally estimated SER, in good agreement with experimental results.

Keywords

Total ionizing dose, X-ray irradiation, soft error rate, synergy effects, alpha particle, single-event upset, fully-depleted silicon-on-insulator, SRAM memory, static noise margin, critical charge, modelling, numerical simulation

Highlights

- Synergy effect of total ionizing dose on alpha-soft error rate in SRAM has been characterized
- Results concern 3 Mbit single-port SRAM powered at 1V in FDSOI 28nm technology
- X-ray irradiation up to 125 krad(Si) have been combined with SER measurements using a ^{241}Am source
- SER degradation is linked to SRAM static noise margin reduction that induces critical charge decrease
- 15% reduction of the critical charge at 125 krad(Si) results in doubling the alpha-soft error rate

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1. Introduction

Total ionizing dose (TID) is known to enhance the susceptibility of circuits to single-event effects (SEE) by modifying the electrical characteristics of individual transistors inside the exposed circuit [1-15]. In the case of static random-access memories (SRAMs), the radiation-induced defects and trapped charges, mainly in oxide and dielectric layers and at their interfaces with the semiconductor, alter the electrical conditions within the SRAM cells, affecting transistor threshold voltages and consequently SRAM stability. The degradation of this latter results in a reduction of the static noise margin (SNM) – the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell – and, consequently, in the reduction of the critical charge (Q_{crit}) – the minimum charge deposited by a ionizing particle at one of the nodes necessary to flip the state of the cell [16-17] – of the SRAM circuit, as shown in some previous studies [8-15].

These synergy effects between TID and single-event effects in devices and circuits are fundamental to apprehend electronic reliability in various environments, like space, accelerators, or future power fusion reactors. In such complex radiation environments, equipment or payloads are or will be subjected to both TID and SEE at the same time, which leads to combined effects on the electronics. However, radiation qualification procedures often perform separate characterizations and, consequently, are not able to catch the underlying physical mechanisms responsible of dose-enhancement SEE sensitivity or other effects [11].

In this work, we experimentally investigate synergy effects between TID and alpha-particle SER in FDSOI 28nm SRAM combining the use of a ^{241}Am solid source and 10 keV X-ray irradiation machine to successively degrade and evaluate the circuit response. The key objective of this study is to model and simulate such effects, step by step, from individual transistor threshold voltage variations to SRAM SER, evaluating the cell stability in terms of static noise margin, critical charge, and finally soft error rate. The paper is organized in two main parts: we describe in Section 2 the circuit under test and the irradiation test setups and procedures, as well as the experimental results. In Section 3, modelling and simulation aspects are presented and used to reproduce experimental data.

2. Experiments

2.1. SRAM test vehicle

In this study, we used a dedicated test vehicle (ANYA_D) manufactured by STMicroelectronics using a commercial ultra-thin body and buried oxide (UTBB) fully-depleted silicon-on-insulator (FDSOI) CMOS 28 nm technology. The UTBB-FDSOI uses a 28 nm high- κ metal-gate, the silicon layer is 7 nm thick on top of an ultra-

thin buried oxide of 25 nm. Details can be found in [18-20], including process description, electrical performances and single event test results for the terrestrial radiation environment (alphas and neutrons). ANYA_D embeds several SRAMs cuts of various densities and power features (Fig. 1). For the purposes of the study, we performed all our measurements on a 3 Mbit single-port high-density (SPHD) SRAM cut powered at $V_{DD} = 1$ V. The circuit schematic of the corresponding SPHD SRAM cell with transistor layout dimensions is given in Fig. 2.

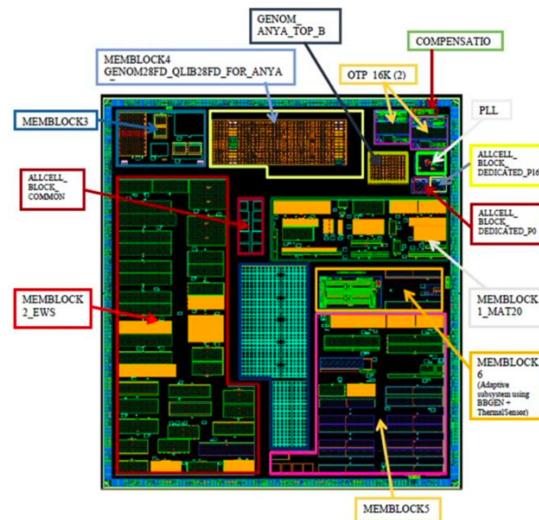


Figure 1. GDS view of ANYA_D test vehicle.

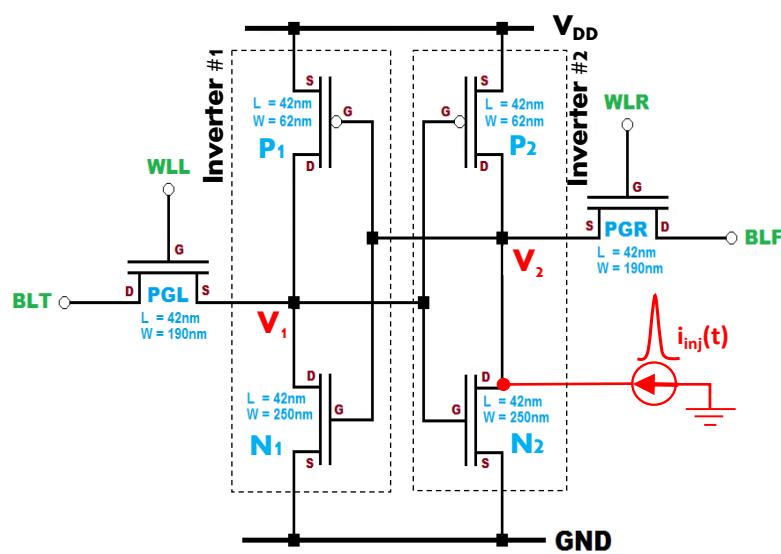


Figure 2. Circuit schematic of the single-port high-density (SPHD) SRAM cell.

2.2. Experimental setups

For the purpose of the study of synergy effects, we designed, constructed and operated a complete experimental setup for both α -SER and TID measurements. This setup consists of a vacuum chamber (bell jar) in which a circuit tester can be operated under a primary vacuum (10^{-2} mbar), in order to maintain the energy of alpha-particles emitted by the source at the level of the entry face of the circuit. The circuit test is a custom tester developed by EASII-IC composed of a main motherboard and one or several test boards. The design of both the hardware and software components of the system follows all the specifications of the JEDEC SER test standard [16]. Each ANYA_D device under test (DUT) is soldered on a DUT test board directly connected to the motherboard. No other active device is present on the test board excepting the tested DUT. The motherboard itself is based on a Xilinx Virtex5 FPGA with embedded memory and a PXA270 processor with Ethernet TCP/IP stack protocol connection. The tester embeds an internal soft error scrubbing code in order to detect internal soft errors. This tester is fully connected to the exterior via vacuum connectors. A power supply with a remote voltage sensing probe is connected to the mother board, as close as possible to the devices. It allows the monitoring of the current consumption of the devices. The measurements are performed independently per power supply line. Fig. 3 shows the experimental setup in irradiation configuration with an ^{241}Am solid source placed in front of a single decapsulated ANYA_D circuit, ready to characterize. Setup of Fig. 3 was used to performe the α -SER characterization of the circuit under test. After exposing the DUT to the alpha source and initializing the SRAM memory plan with a checkerboard test pattern, the tester searches for errors in loop in the SRAM array until the test sequence is terminated.

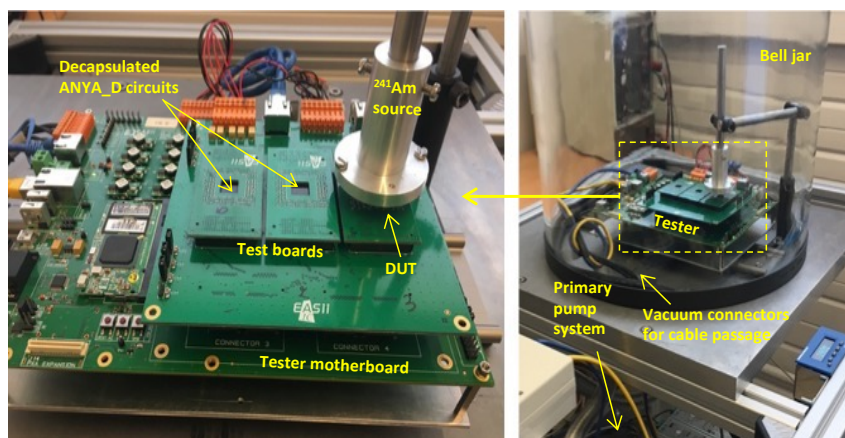


Figure 3. Alpha-particle irradiation setup using a ^{241}Am solid source (4 kBq in 2π sr) and a vacuum bell jar. All circuit connections go through vacuum connectors, allowing real-time measurements during irradiation.

After this measurement step, the tester itself with the circuit was moved to the X-ray irradiation setup (Fig. 4) for irradiation at a dose rate of 100 rad(Si)/s. During X-ray irradiation, the SRAM memory plan was maintained initialized with the same checkerboard test pattern as used during α -irradiation.

Repeating the cycle (α -SER measurement + X-ray irradiation) for different values of the TID allows us to characterize synergy effects between SER and TID from 0 to 128 krad(Si).

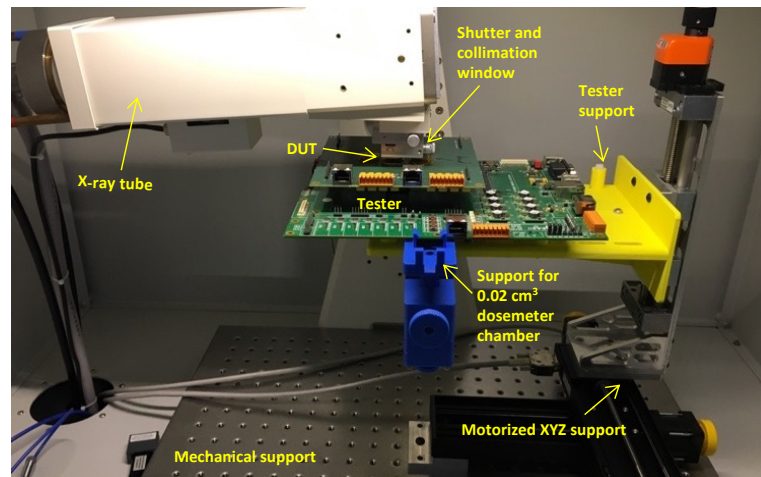


Figure 4. X-ray irradiation setup using a 10 keV X-ray tube with a tungsten cathode (for clarity, the circuit tester is not connected).

2.3. α -SER versus TID experimental results

Figure 5 shows the cumulated number of bit flips detected during α -irradiation as a function of measurement time before (fresh) and after X-ray irradiation that corresponds to the maximum dose of 128 krad(Si) for which the circuit is fully functional. Note the surprisingly long duration of the experiments (up to 7 hours) for such accelerated tests using a source with 4 kBq of activity: this is due to the relative immunity of FDSOI architectures to single events, characterized by very low SER values [19-20], reported in Fig. 5. In this sense, the curves of Fig. 5 resemble those of real-time SER experiments, but with a different abscissa, expressed in hours and not in months or years of exposure to radiation [21-23]. The two distribution slopes of Fig. 5 are directly linked to the α -SER: after 128 krad(Si), the slope (and thus the SER) is quasi twice that of the distribution before irradiation, demonstrating the TID synergy effect on the circuit SER. It must be noted at this level that the magnitude of the SER degradation may depend on the test patterns applied during TID and alpha-particle irradiation sequences [24] but this effect is out of the scope of our study.

In the following, our objective is to step-by-step retrieve by simulation and confirm this measured SER from the TID response of both NMOS and PMOS transistors, elements of the SRAM cell.

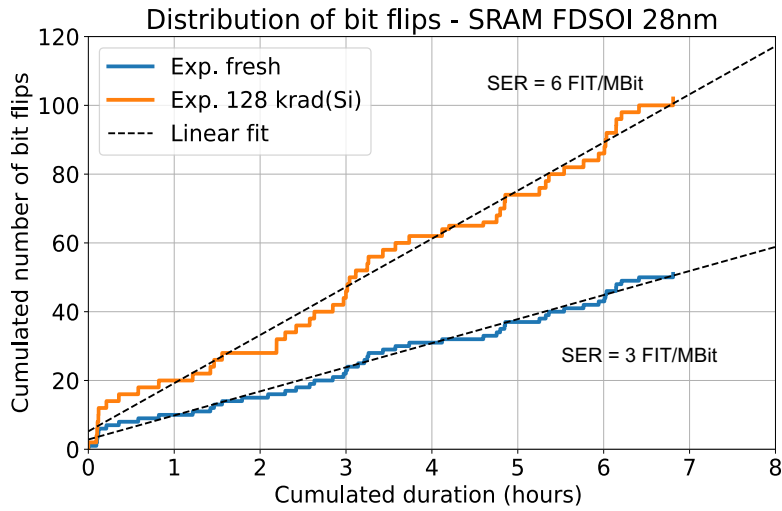


Figure 5. Cumulated number of bit flips in 3 Mbit SRAM cut ($V_{CC} = 1$ V) as a function of the α -irradiation time before (fresh) and after 128 krad(Si) X-ray irradiation of the circuit. The corresponding SER (FIT/Mbit) is calculated for an α -emissivity of 10^{-3} $\alpha/cm^2/h$. For industrial confidentiality reason, all SER results have been normalized by a common arbitrary scaling factor.

2.4. TID characterization of individual transistors

In complement to SER versus TID experiments, we performed electrical characterization of individual transistors for the extraction of the threshold voltage shift as a function of TID. Figure 6 shows the $I_D(V_G)$ characteristics before irradiation and after 128 krad(Si) for both NMOS and PMOS individual transistors. ΔV_T is negative since the radiation-induced trapped charges are mainly positive whatever the type of the transistor [7]. ΔV_T versus TID (Fig. 7) are also more important in absolute value for NMOS than for PMOS. The latter appear to be less TID-sensitive than NMOS, as already shown [25].

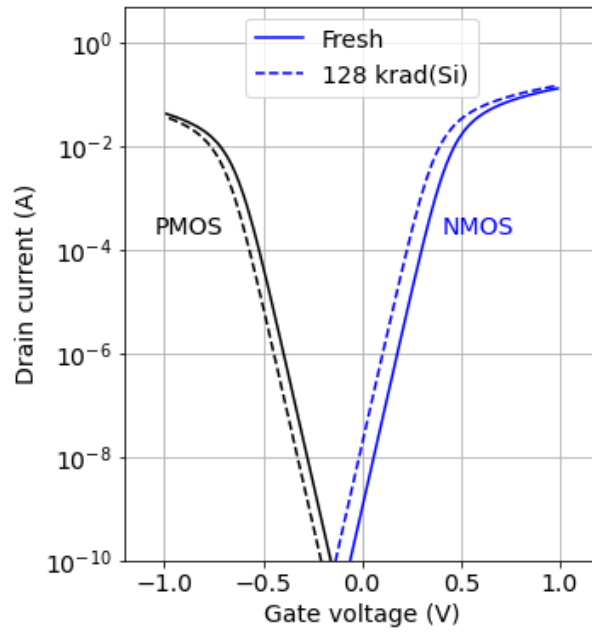


Figure 6. $I_D(V_G)$ characteristics before (fresh) and after 10 keV X-ray irradiation at 128 krad(Si) for both NMOS and PMOS transistors ($L = 42$ nm, $W = 1$ μm).

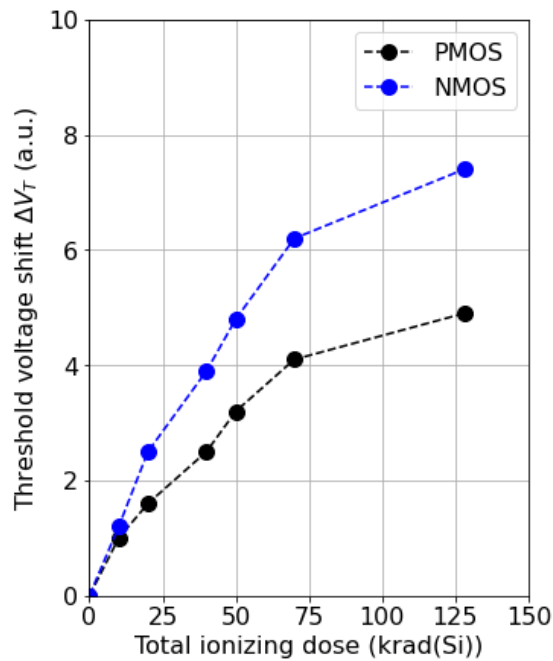


Figure 7. Negative threshold voltage shifts versus TID extracted from $I_D(V_G)$ curves for both NMOS and PMOS transistors. For industrial confidentiality reason, all values have been normalized by a common arbitrary scaling factor.

3. Modelling and simulation

3.1 Transistor and SRAM modelling

We implemented in C++ the UTSOI model (v1.1.4) developed by the CEA-LETI (and initially in the form of Verilog-A(MS) source code) for ultra-thin fully depleted SOI MOSFET [26]. This surface potential model was implemented under the form of two numerical functions $I_{DN}(V_G, V_D)$ and $I_{DP}(V_G, V_D)$ returning the source-to-drain current for NMOS and PMOS transistors, respectively, with V_G and V_D the applied voltages on the gate and drain terminals, respectively (here $V_S = V_B = 0$ V for source and bulk terminals). In this model, the source-to-drain current expression is obtained by a similar equation as in PSP model [27]:

$$I_D = WC_{ox}\mu\frac{kT}{q}\left[\int_{x_{n,s}}^{x_{n,d}}q_id x_n - \int_{q_{i,s}}^{q_{i,d}}dq_i\right] \quad (1)$$

where C_{ox} is the gate oxide capacitance per unit area, q_i is the inversion charge, μ is the carrier mobility, W is the channel width, $x_{n,d}$ and $x_{n,s}$ are the quasi Fermi levels at the drain and source sides respectively, $q_{i,d}$ and $q_{i,s}$ are the inversion charges at the drain and source sides, respectively.

Note that the integral terms in Eq. (1) depend, among other parameters, on the channel length L and on the transistor threshold voltage V_T , that do not explicitly appear in this formulation. Eq. (1) can be expressed analytically considering a series of developments and approximations described in [28]. It has been used in our standalone SRAM cell simulator [29-30] for time-domain transient simulation and for the determination of the static noise margin (SNM) and critical charge Q_{crit} , as explained in the following. Considering the storage node of the SRAM cell of Fig. 2 composed of the two cross-coupled inverters #1 and #2, the time variations of the node voltages V_1 and V_2 are solutions of the system of two coupled differential equations:

$$\begin{cases} \frac{dV_1}{dt} = \frac{I_{DP1}(V_2-V_{DD}, V_1-V_{DD}) - I_{DN1}(V_2, V_1)}{C_N} = F(t, V_1, V_2) \\ \frac{dV_2}{dt} = \frac{-i_{inj}(t) + I_{DP2}(V_1-V_{DD}, V_2-V_{DD}) - I_{DN2}(V_1, V_2)}{C_N} = G(t, V_1, V_2) \end{cases} \quad (2)$$

where index 1 and 2 refer to the two inverters of the SRAM cell (defined in Fig. 2), C_N is the storage node capacitance (determined from technological process and layout proprietary information), $i_{inj}(t) = 0$ for the determination of the static noise margin of the SRAM cell and $i_{inj}(t)$ is given by Eq. (8) (see section 3.3.)

This system of differential equations can be easily solved in the time domain, using a 4th order Runge-Kutta method [31] with a time step Δt . Using notations introduced in Eq. (2), the incremental results for $t_{n+1} = t_n + \Delta t$ are:

$$\begin{cases} V_1^{n+1} = V_1^n + \frac{K_1 + 2K_2 + 2K_3 + K_4}{6} \\ V_2^{n+1} = V_2^n + \frac{L_1 + 2L_2 + 2L_3 + L_4}{6} \end{cases} \quad (3)$$

with:

$$K_1 = F(t^n, V_1^n, V_2^n)\Delta t \quad L_1 = G(t^n, V_1^n, V_2^n)\Delta t \quad (4)$$

$$K_2 = F(t^n + \frac{\Delta t}{2}, V_1^n + \frac{K_1}{2}, V_2^n + \frac{L_1}{2})\Delta t \quad L_2 = G(\dots)\Delta t \quad (5)$$

$$K_3 = F(t^n + \frac{\Delta t}{2}, V_1^n + \frac{K_2}{2}, V_2^n + \frac{L_2}{2})\Delta t \quad L_3 = G(\dots)\Delta t \quad (6)$$

$$K_4 = F(t^n + \frac{\Delta t}{2}, V_1^n + K_3, V_2^n + L_3)\Delta t \quad L_4 = G(\dots)\Delta t \quad (7)$$

where the argument for G in the second member of these equations is the same as for F.

Equations (3) to (7) constitute the core model for solving the time evolution of the SRAM cell node voltages. For the static noise margin determination, each differential equation of (2) can be solved separately, imposing a voltage sweep from 0 to V_{DD} for the voltage of the second node.

3.2. Static noise margin

Figure 8 shows the computed SRAM “butterfly” curves before and after several doses, up to 128 krad(Si). The effect of the dose on the reduction of the static noise margin, taken into account via the ΔV_T values for both PMOS and NMOS transistors of the SRAM cell, is clearly visible. For memory, the SNM is defined as the side length of the largest square that can be fitted inside the lobes of the “butterfly” curve. Figure 8 evidences the closing of the curves, quantified in Fig. 9 in terms of SNM values. At 128 krad(Si), SNM is reduced to about 20% with respect to the value before irradiation.

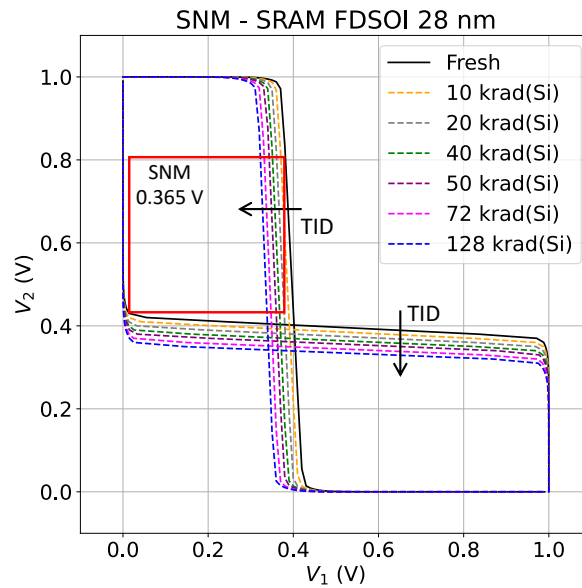


Figure 8. Simulated SRAM cell “butterfly” curves before and after irradiation at several TID values. SNM is graphically extracted here for the curve before irradiation (fresh).

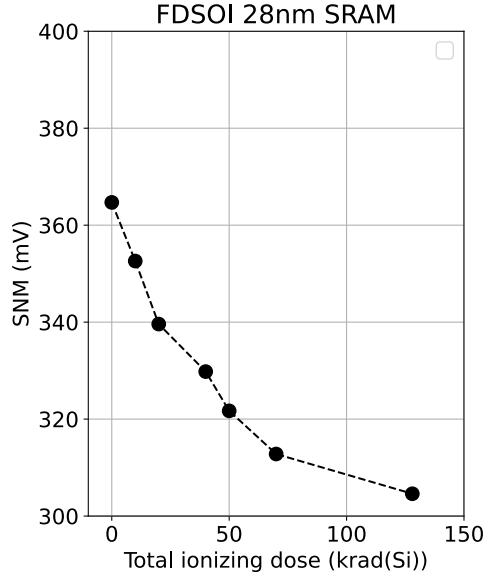


Figure 9. SNM versus TID for the FDSOI 28 nm SPHD SRAM cell defined in Fig. 2 and extracted from numerical simulation shown in Fig. 8.

3.3. Critical charge

The decrease in stability of the SRAM cell, evidenced by the SNM reduction, has a direct impact on its susceptibility to single events. For simulating such events at circuit level, we solve this time the full system of equations (2) considering the variations of the transistor threshold voltages in both I_{DN} and I_{DP} calculation functions and a double exponential current transient pulse $i_{inj}(t)$ injected on the struck node #2 (see Fig. 2) during the transient simulation [32]:

$$i_{inj}(t) = \frac{Q}{t_f - t_r} [\exp(-t/t_f) - \exp(-t/t_r)] \quad (8)$$

where Q is the collected charge on the struck node (i.e., the integral of the pulse), t_r is the rising time constant, and t_f is the falling time constant. Slowly varying Q around the stability point of the SRAM cell allows us to determine the critical charge for a given TID value, as illustrated in Fig. 10 for the fresh cell. Figure 11 shows the decrease of Q_{crit} with TID, as deduced from the above circuit simulation. The normalized $Q_{crit}(D)/Q_{crit}(0)$ variation with the total ionizing dose D (expressed in krad(Si)) is empirically well described by an exponential law under the form:

$$Q_{crit}(D)/Q_{crit}(0) = A + B \times \exp(-\lambda D) \quad (9)$$

where parameters $A = 0.83$ (unitless), $B = 0.167$ (unitless) and $\lambda = 0.02 \text{ krad(Si)}^{-1}$.

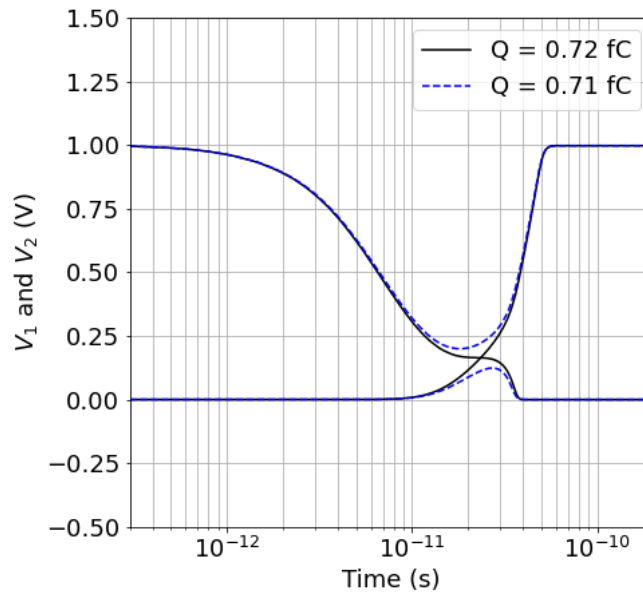


Figure 10. Transient simulation of the SRAM cell (before irradiation) subjected to a particle strike mimicked by (8) with two values of Q . V_1 and V_2 correspond to the potentials of the two storage nodes of the cell.

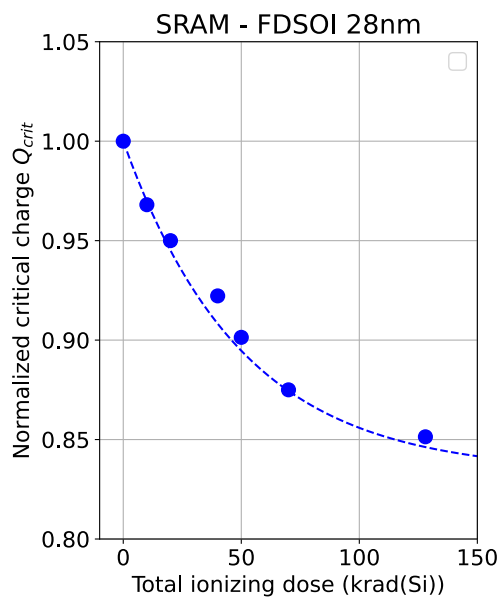


Figure 11. Critical charge versus TID extracted from transient simulation considering a double exponential current pulse.

3.4. Soft error rate

The decrease of Q_{crit} versus TID highlighted in Fig. 11 logically leads to an increase of the SER with TID, as evidenced in Fig. 12. In this figure, experimental SER data have been obtained from the cumulated distributions of bit flips as a function of the α -irradiation time (see Fig. 5) for the different TID values (remember that the

extracted SER values expressed in FIT/Mbit are calculated for an α -emissivity of $10^{-3} \alpha/\text{cm}^2/\text{h}$. Experimental results show that the SER is multiplied by a factor of two by a total ionized dose of 125 krad(Si). This evolution of the SER values with TID is not linear and can be nicely described with the Hazucha and Svensson's equation for the SER [33]:

$$SER = K \times \exp(-Q_{crit}/Q_s) \quad (10)$$

where the prefactor K and the collection efficiency Q_s are two fitting parameters and Q_{crit} values correspond to data of Fig. 11.

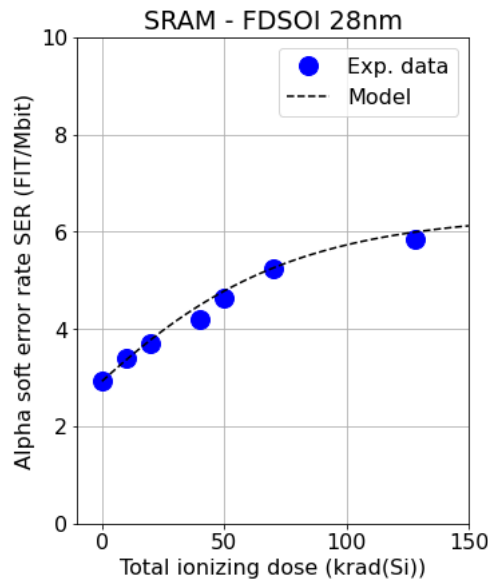


Figure 12. Alpha soft error rate versus TID for the FDSOI 28 nm SPHD SRAM as deduced from experimental data of Fig. 5 and from Eq. (10) using Q_{crit} values of Fig. 11.

The best fit of Eq. (10) on SER data is obtained with $K = 310$ FIT/Mbit and $Q_s = 0.154$ fC, as illustrated in Fig. 12. The behavioural modelling predicted by this equation is an important quantitative information that can be imported in design for reliability tools used to size electronic systems containing the characterized memory for a given mission profiles, for example for space applications.

4. Conclusion

In conclusion, we investigated the synergy effect of total ionizing dose on alpha-soft error rate paper in a 3 Mbit SRAM test circuit manufactured by STMicroelectronics in CMOS 28nm FDSOI technology. This work is original for this technology and self-consistent in so far as it clearly details the methodology and gives all the equations, models and calculation steps to relate the performance of individual transistors to the response of the SRAM cell, from an electrical stability and soft-error rate points of view. Synergy effects were experimentally characterized using a circuit tester alternatively embedded in vacuum chamber for alpha-particle irradiation using a ^{241}Am solid source and in an irradiation machine for 10 keV X-ray exposure. Total ionizing doses up to 125 krad(Si) have been performed and their impact on the α -SER has been characterized from the cumulated number of bitflips as a function of the exposition time to the alpha-source detected on a 3 Mbit single-port SRAM cut powered at 1V. Our experimental result showed that a 15% reduction of the critical charge at 125 krad(Si) results in doubling the alpha-soft error rate from 3 to 6 FIT/Mbit. Modelling and simulation of the storage element (double inverter) of a single SRAM cell was conducted, considering a dedicated and characterized FDSOI transistor model (UTSOI v.1.1.4) and a double exponential current transient pulse to emulate the impact of alpha-particles on the SRAM sensitive node. Simulation results quantitatively link transistor threshold voltage variations to SRAM cell stability in terms of static noise margin and critical charge. The estimated reduction of the soft error rate was found in excellent agreement with experimental results, demonstrating that such a behavioural modelling can be used for reliability prediction of this FDSOI SRAM technology, considering a given mission profiles combining TID and single event constraints, for example for space applications.

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