Understanding evolving risks of single event effects

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Abstract

This short-course surveys the status of recent research works in the domain of single event effects (SEE) in advanced CMOS technologies, such as fully depleted silicon-on-insulator (FD-SOI), FinFET, tri-gate or multi-gate configurations based on ultra-thin films or nanowire channels. This review primarily focus on the understanding of evolving risks related to SEE in such a "More Moore" roadmapping effort, mainly driven by an extreme geometrical scaling of devices and a concomitant supply voltage reduction. Some important key-points are particularly presented and discussed: the critical charge and ion-track spatial structure vs. device feature sizes, the impact of variability on SEE, the increasing sensitivity to background radiation (including the emerging issues of terrestrial muons and alpha-particles from traces of contaminants in device, circuit and packaging materials), the emergence of new physical mechanisms in advanced technologies (e.g. bipolar amplification). Finally, the review briefly discusses the SEE sensitivity of a few "More than Moore" CMOS solutions envisaged for 3D integration of future circuits.

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1 Introduction

1.1 Background

Microelectronics industry has experienced tremendous progress in the last forty years, especially with regard to the evolution of the products (i.e. integrated circuits) performances, and at the same time, concerning the drastic reduction of manufacturing costs by elementary integrated function. So far, this considerable growth of the semiconductor industry has been due to its technological capability to constantly miniaturize the elementary components of circuits, namely the MOSFET (metal-oxide-semiconductor field effect transistor), the basic building block of VLSI (very large scale integration) integrated circuits. The continuous decrease of the silicon surface occupied by these elementary components has kept the race integration at the rhythm dictated by the famous “Moore's Law”, which states that the number of transistors per integrated circuit doubles every 18 to 24 months [1]. However, the conventional bulk MOSFET scaling down encountered this last decade serious physical and technological limitations, mainly related to the gate oxide (SiO_2) leakage currents [2-3], the large increase of parasitic short channel effects and the dramatic mobility reduction [4] due to highly doped silicon substrates precisely used to reduce these short channel effects. Technological solutions have been proposed in order to continue to use the “bulk solution” until the 32-28 nm ITRS nodes [5]. Most of these solutions have then introduced high-permittivity gate dielectric stacks (to reduce the gate leakage, [1], [6], midgap metal gate (to suppress the Silicon gate polydepletion-induced parasitic capacitances) and strained silicon channel (to increase carrier mobility) [7]. However, in parallel to these efforts, alternative solutions to replace the conventional bulk MOSFET architecture have been proposed and studied in the recent literature. These options are numerous and can be classified in general according to three main directions: (i) the use of new materials in the continuity of the “bulk solution”, allowing increasing MOSFET performances due to their dielectric properties (permittivity), electrostatic immunity (SOI materials), mechanical (strain), or transport (mobility) properties; (ii) the complete change of the device architecture (e.g. Multiple-Gate devices, Silicon nanowires MOSFET) allowing better electrostatic control, and, as a result, intrinsic channels with higher mobilities and currents; (iii) the exploitation of certain new physical phenomena that appear at the nanometer scale, such as quantum ballistic transport, substrate orientation or modifications of the material band structure in devices/wires with nanometer dimensions [8-9].

As the MOSFET is scaling down, the sensitivity of the integrated circuits to radiation coming from the natural space or present in the terrestrial environment has been found to seriously increase [10-13]. In nowadays ultra-scaled devices, the natural radiation is inducing one of the highest failure rates of all reliability concerns for devices and circuits entering in the area of nanoelectronics [5],[14]. In particular, ultra-scaled memory integrated circuits have been found to be more sensitive to single-event-upset (SEU) and digital devices more subjected to digital single-event transient (DSETs). This sensitivity is a direct consequence of the reduction of device dimensions and spacing within memory cells combined with the reduction of supply voltage and node capacitance, resulting in a decrease of both the critical charge (i.e. the minimum amount of charge required to induce the flipping of the logic state) and the sensitive area (i.e. the minimum collection area inside which a given particle can deposit enough charge to induce the flipping of the cell) [13-15].

1.2 Objective

The objective of this short-course is to offer a survey of the most recent research works in the domain of single event effects (SEE) in advanced CMOS technologies, such as fully depleted silicon-on-insulator (FD-SOI), FinFET, tri-gate or multi-gate configurations based on ultra-thin films or nanowire channels. The review will focus on the understanding of evolving risks related to SEE in such a “More Moore” roadmapping effort, mainly driven by an extreme geometrical scaling of devices and a

concomitant supply voltage reduction. The survey will conclude on the first works related to the SEE sensitivity of a “More than Moore” near-term perspective concerning the 3D integration of future circuits.

1.3 Structure and scope

This short-course is structured in three main parts. In part II, we will introduce the essential notions related to the main mechanisms of SEE in microelectronics devices and circuits. In this part several introductory subjects will be briefly reminded such as the description of radiation environments vs. application issue (space, atmospheric and ground level), the particle-matter interactions (including the atmospheric radiation environment and telluric sources), and the SEE production mechanisms in silicon devices (including SEU mechanisms in memory circuits). Part III will explain how to estimate SEE from device to circuit level and from engineering approaches to very detailed models. We will also discuss what are the advantages and inconvenient of these methods. Part IV will present and discuss the main SEE trends versus smaller feature sizes; it will also address the problem of the increasing sensitivity to background radiation in the terrestrial environment or caused by the presence of ultra-traces of radioactive contaminants in device/circuit/packaging materials. Finally, the end of Part IV will be dedicated to emerging devices and related physical mechanisms concerning the radiation sensitivity of several important “More Moore” and "More than Moore" issues.

2 Brief overview of basic SEE phenomena

2.1 Radiation environments vs. applications (space, atmospheric and ground level)

Single event effects (SEE) are the result of the interaction of highly energetic particles, such as protons, neutrons, alpha particles, or heavy ions, with the sensitive region(s) of a microelectronic device or circuit. A single event may perturb the device/circuit operation (e.g., reverse or flip the data state of a memory cell, latch, flip-flop, etc.) or definitively damage the circuit (e.g. gate oxide rupture, destructive latch-up events). The problem has been well known for space applications over many years (more than forty years) and production mechanisms of SEE in semiconductor devices by protons or heavy ions well apprehended, characterized and modeled [16]. In a similar way for avionic applications, the interaction of atmospheric neutrons (and to a lesser extend protons) with electronics has been identified as the major source of SEE [17]. For the most recent deca-nanometers technologies, the impact of other atmospheric particles produced in nuclear cascade showers on circuits has been clearly demonstrated, in particular low energy protons [18-19] and more recently atmospheric low energy muons [20-24]).

With respect to such high-altitude atmospheric environments, the situation at ground level is slightly different. Of course, atmospheric neutrons are always the primary particles but, with a flux approximately divided by a factor ~300 at sea-level with respect to the flux at avionics altitudes, the soft error rate (SER) of circuits can be now affected by other additional sources of radiation: the alpha particles generated from traces of radioactive contaminants in CMOS process or packaging materials [25-26] and the low energy atmospheric muons. As a consequence of these multiple sources of radiation, the accurate modeling and simulation of the SER of circuits at ground level is rather a complex task because one can clearly separate the contribution to SER of atmospheric particles (the external constraint) from the one due to natural alpha-particle emitters present as contaminants in circuit materials (the internal constraint).

2.2 Main sources of natural radiation at ground level

As briefly stated before, natural radiation that causes soft error in digital circuits may come from various sources. At ground level, one can distinguish two major sources of

radiation described in the following: i) the atmospheric radiation environment and ii) the telluric radiation sources.

2.2.1 Atmospheric radiation

A complex cascade of elementary particles and electromagnetic radiation is generally produced in the Earth's atmosphere when a primary cosmic ray (of extraterrestrial origin) interacts with the top atmosphere [27]. The term cascade means that the incident particle (generally a proton, a nucleus, an electron or a photon) strikes a molecule in the air so as to produce many high energy secondary particles (photons, electrons, hadrons, nuclei) which in turn create more particles, and so on.

Among all these produced secondary particles, neutrons represent the most important part of the natural radiation constraint at ground level susceptible to impact current electronics. Because neutrons are not charged, they are very invasive and can penetrate deeply in circuit materials. They can interact via nuclear reactions with the atoms of the target materials and create (via elastic or inelastic processes) secondary ionizing particles. This mechanism is called "indirect ionization" and is potentially an important source of errors induced in electronic components. One generally distinguishes thermal neutrons (interacting with ^{10}B isotopes potentially present in circuit materials, but progressively removed from technological processes [13]) and high-energy atmospheric neutrons (up to the GeV scale). Figure 1 (top) shows the typical energy distribution of atmospheric neutrons, ranging from thermal energies to 1 GeV, as experimentally measured by Gordon, Goldhagen et al. [28] using a Bonner multi-sphere spectrometer at the reference location (New-York City, NYC). The integration of this spectrum, also shown in Figure 1 (bottom), gives the total neutron flux expressed in neutrons per square centimeter and per hour: this flux is equal to 7.6 n/cm^2/h for the lower part (thermal and epithermal neutrons below 1 eV), 16 n/cm^2/h for the intermediate part (between 1 eV and 1 MeV) and 20 n/cm^2/h for the upper part (high energy neutrons above 1 MeV). This last value is reduced to 13 n/cm^2/h when integrating the flux above 10 MeV.

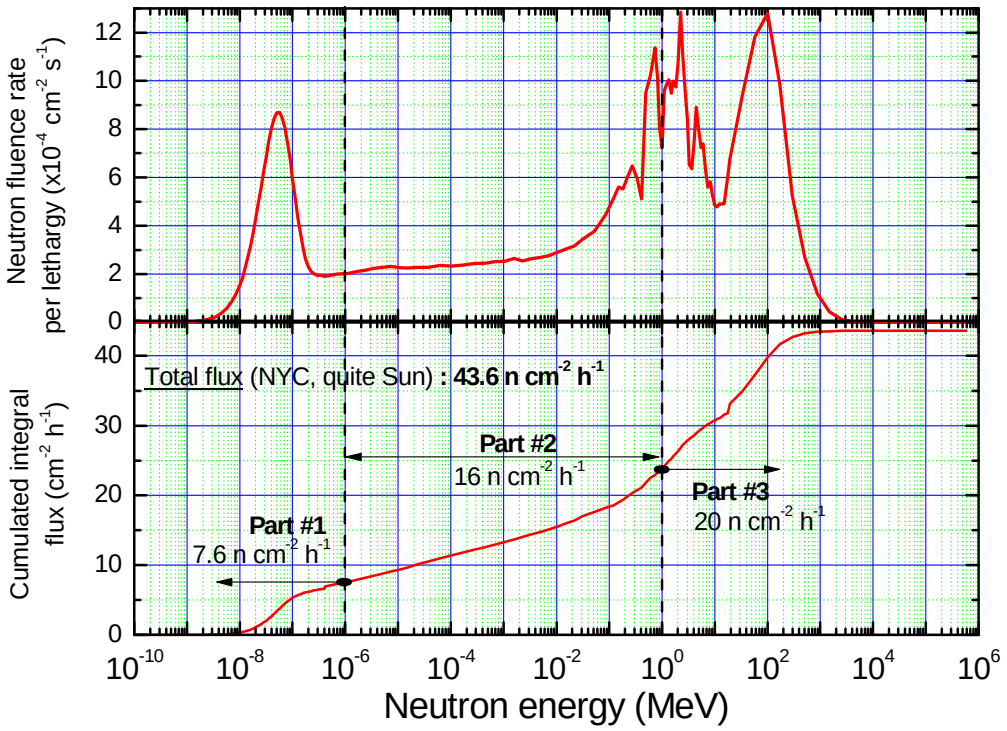


Figure 1: Top: Reference atmospheric neutron spectrum measured on the roof of the IBM Watson Research Center main building [28]. Numerical data courtesy from Paul Goldhagen (U.S. Department of Homeland Security). Bottom: Cumulated integral flux corresponding to the above spectrum. The total neutron flux is 43.6 neutrons per cm^2 and per hour.

Atmospheric muons also represent an important part of the natural radiation constraint at ground level [27]. But despite this abundance, muons interact extremely few with matter, excepted at low energies (typically in the 1-10 MeV energy range) by direct ionization. The relative importance of low energy muons in the SER of the most advanced CMOS technologies will be discussed in details in paragraph 4.3.2.

In contrast and while strongly interacting with matter, pions are not enough abundant at ground level to induce significant effects in components. Furthermore, for modern technologies, the small amount of electrons and gamma rays with low energies (susceptible to interact with matter) are not able to disrupt electronics.

Finally, protons, although they interact with silicon as neutrons above a few tens of MeV, are one hundred times less numerous than the latter at ground level. Their low abundance allows us to consider their impact as negligible compared to that of neutrons, except at low energies (< 1 MeV) for which certain advanced technologies show an exacerbated sensitivity due to charge deposition by direct ionization.

Figure 2 shows a typical energy distribution of the differential flux for atmospheric neutrons, protons, muons and pions at ground level. Such a collection of spectra, characteristic of a given location (latitude, longitude and elevation), constitute a set of input data of primary importance for any simulation code dedicated to the evaluation of the soft error rate induced by the atmospheric radiation environment (see section 4).

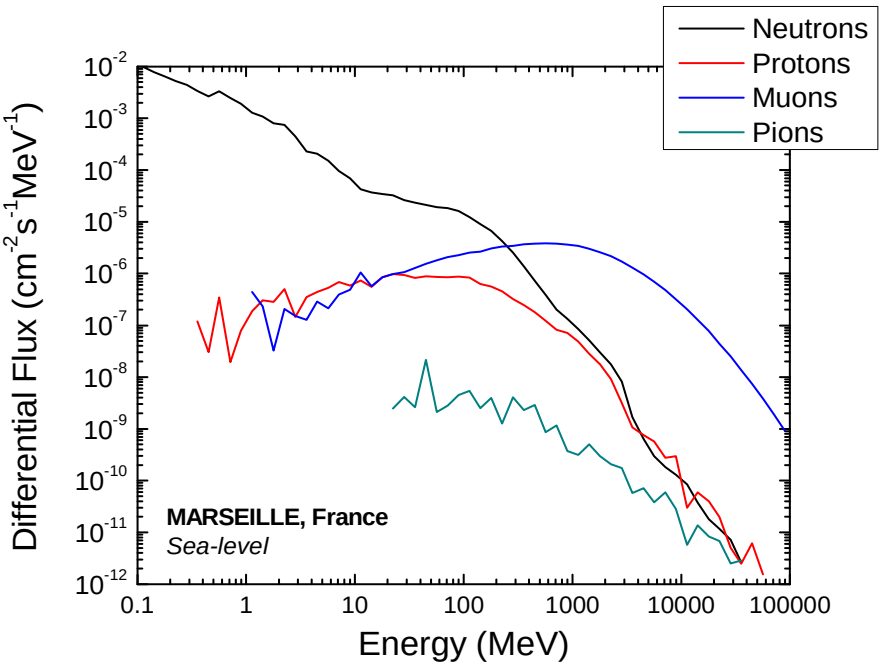


Figure 2: High energy (> 0.1 MeV) differential flux for atmospheric neutrons, protons, muons and pions at ground level. Data computed using the Qinetic Atmospheric Radiation Model [29-30] for Marseille, France (Latitude 43.18' N, Longitude 5.22' E, sea-level).

2.2.2 Telluric radiation sources

Every terrestrial material contains traces of radioactive atoms, in a wide range varying from a few atoms on thousands for the most active materials to a few atoms on tens of billions for the most purified ones. These natural radioisotopes contained in the Earth's crust are the principal natural sources of α, β and γ radioactivity but only the alpha-particle emitters present a reliability concern in microelectronics. Beta and gamma processes are indeed not able to deposit a high enough amount of energy susceptible to significantly impact the microelectronic circuit operation. On the contrary, alpha-particles (He^{2+}) produced by radioactive decay with typical energies ranging from 1 to 10 MeV can cause a sudden burst of several millions of electrons in silicon over a path of a few tens of microns. This is largely sufficient to induce a transient current susceptible to disturb the operation of a given integrated circuit, as we will illustrate later in this course.

As clarified by Wrobel et al. [31], these radioactive nuclei can be classified into two categories: the “radioactive materials” and the “radioactive impurities” or pollutants. Radioactive materials naturally contain a proportion, generally weak, of alpha-emitter isotope, as for example hafnium (^{174}Hf is an alpha emitter, its natural abundance is 0.162%). The second category corresponds to an unwanted element, i.e. unintentionally introduced during the process. This mainly corresponds to uranium and thorium, which have alpha emitter isotopes in their respective disintegration decay chain (see below). ^{232}Th and ^{238}U are widely present in the natural environment and can easily pollute water flow and raw materials used at wafer, packaging and interconnection levels.

Considering the activity of radioisotopes in the calculation of the soft error rate of a circuit thus requires to accurately modeling the alpha-particle source mimicking the presence of these alpha-particle emitters in the circuit materials. For example, considering traces of uranium in a given material (silicon for example) requires taking into account the complete uranium disintegration chain composed of 14 daughter nuclei with 8 alpha-particle emitters. Energies of these alpha particles are ranging from 4.20 to 7.68 MeV; their corresponding ranges in silicon vary from 19 to 46 µm and their initial Linear Energy Transfer (LET) from 0.47 to 0.68 MeV/(mg/cm²), as summarized in Table 1.

	$T_{1/2}$ (s)	Alpha Energy (MeV)	Range in Si (µm)	Corresponding initial LET (MeV/(mg/cm²))
^{238}U	$1.40\times10^{+17}$	4.19	18.95	0.677
^{234}U	$7.76\times10^{+12}$	4.68	22.17	0.634
^{230}Th	$2.38\times10^{+12}$	4.58	21.49	0.642
^{226}Ra	$5.05\times10^{+10}$	4.77	22.78	0.627
^{222}Rn	$3.30\times10^{+05}$	5.49	27.94	0.575
^{218}Po	$1.86\times10^{+02}$	6.00	31.86	0.545
^{214}Po	1.64×10^{-04}	7.68	46.22	0.468
^{210}Po	$1.20\times10^{+07}$	5.31	26.61	0.588

Table 1: Main characteristics (half-life, mean energy, range in silicon and initial linear energy transfer of the emitted alpha-particle) of the eight alpha-emitters of the disintegration chain of ^{238}U [32].

2.3 SEE production at silicon level

The physical mechanisms related to the production of SEE in microelectronic devices schematically consist in three main successive steps: (1) the charge deposition by the energetic particle striking the sensitive region, (2) the transport of the released charge into the device and (3) the charge collection in the sensitive region of the device. Figure 3 illustrates these successive steps in the case of the passage of a high-energy ion through a reverse-biased n+/p junction. In the following, we succinctly describe these different mechanisms, for a detailed presentation we invite the reader to consult ref. [10]-[13].

Charge deposition (or generation): When an energetic charged particle strikes the device, an electrical charge along the particle track can be deposited by one of the following mechanisms: direct ionization by the interaction with the material or indirect ionization, by secondary particles issued from nuclear reactions with the atoms of the struck material. Direct ionization typically characterizes heavy ions ($Z \geq 2$) of the space environment. They interact with the target material mainly by inelastic interactions and transmit a large amount of energy to the electrons of the struck atoms. These electrons produce a cascade of secondary electrons which thermalize and create electron-hole pairs along the particle path [Fig. 3(b)].

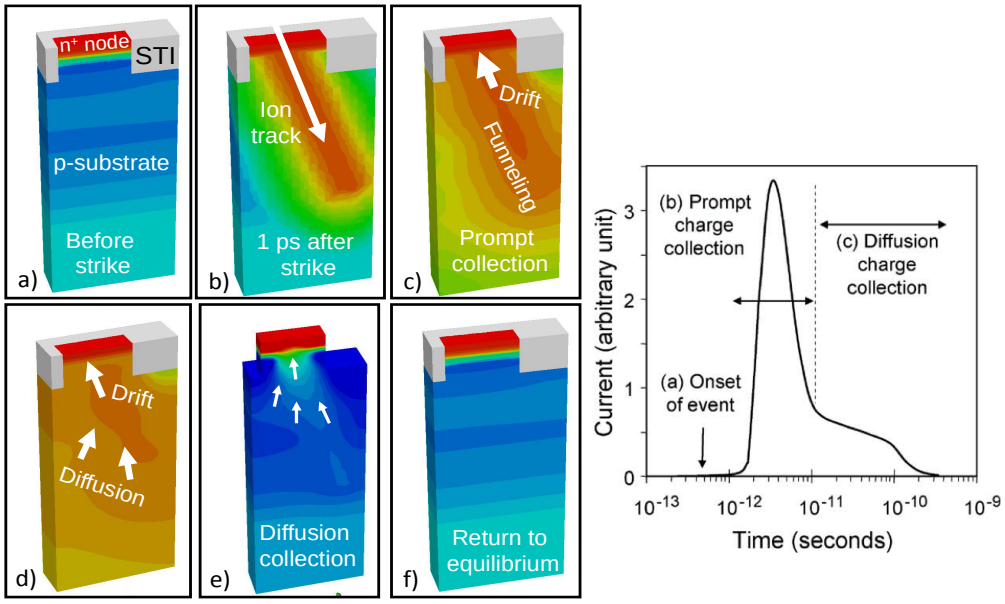


Figure 3: Charge generation, transport and collections phases in a reverse-biased junction and the resultant current pulse caused by the passage of a high-energy ion. TCAD screenshots by courtesy of P. Roche (STMicroelectronics). Drain current transient adapted after Bauman [13]. © 2005 Institute of Electrical and Electronics Engineers Inc.

In a semiconductor or insulator, a large amount of the deposited energy is thus converted into electron-hole pairs, the remaining energy being converted into heat and a very small quantity in atoms displacement. It was experimentally shown that the energy necessary for the creation of an electron-hole pair depends on the material bandgap. In a microelectronics silicon substrate, one electron-hole pair is produced for every 3.6 eV of energy lost by the ion. Other particles, such as the neutrons of the terrestrial environment, do not interact directly with target material since they do not ionize the matter on their passage. However, these particles should not be neglected, because they can produce SEE due to their probability of nuclear reaction with the atoms of materials that compose the microelectronic devices. This mechanism is called indirect ionization. The products resulting from a nuclear reaction can deposit energy along their traces, in the same manner as that of direct ionization. Since the creation of the column of electron-hole pairs of these secondary particles is similar to that of ions, the same models and concepts can be used.

Charge transport: When a charge column is created in the semiconductor by an ionizing particle, the released carriers are quickly transported and collected by elementary structures (e.g. p-n junctions). The transport of charge relies on two main mechanisms [Figs. 3(c) to 3(e)]: the charge drift in regions with an electric field and the charge diffusion in neutral zones. The deposited charges can also recombine with other mobile carriers existing in the lattice.

Charge collection: The charges transported in the device induce a parasitic current transient [Fig. 3 right], which could induce disturbances in the device and associated circuits. The devices most sensitive to ionizing particle strikes are generally devices containing reversely-biased p-n junctions, because the strong electric field existing in the depletion region of the p-n junction allows a very efficient collection of the deposited charge. The effects of ionizing radiation are different according to the intensity of the current transient, as well as the number of impacted circuit nodes. If the current is sufficiently important, it can induce a permanent damage on gate insulators (gate rupture, SEGR) or the latch-up (SEL) of the device. In usual low power circuits, the transient current may generally induce only an eventual change of the logical state (cell upset).

2.4 SEE terminology (SET, SEFI, SEL, SEGR, SEU, SER)

As defined by the JEDEC standard JESD89A [33], JESD57 [34] and ESCC25100 [35], single event effects indicate any measurable or observable change in state or

performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike. Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET), single-event burnout (SEB) and single-event gate rupture (SEGR). The soft error rate (SER) indicates the rate at which soft errors occur. We precise in the following the most important terms and related definitions:

- **Soft error**: An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell. As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process. Soft errors can be generated from SEU, SEFI, MBU, MCU, and or SET. The term SER has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc. are typically used by the avionics, space and military electronics communities. Historically, the term “soft error” was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term “single event upset” was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).
- **Single-event upset (SEU)**: A soft error caused by the transient signal induced by a single energetic particle strike.
- **Single-event upset (SEU) cross-section**: The number of events per unit fluence. For device SEU cross-section, the dimensions are sensitive area per device. For bit SEU cross-section, the dimensions are area per bit.
- **Single-event upset (SEU) rate**: The rate at which single event upsets occur.
- **Single event transient (SET)**: A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by a single energetic particle strike.
- **Single-event latch-up (SEL)**: An abnormal self-sustainable high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality. SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation. An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic thyristor structure (p-n p-n) shorting of power to ground.
- **Single-event gate rupture (SEGR)**: Total or partial damage of the dielectric gate material due to an avalanche breakdown.

In addition to the previous terminology, we mention here, for memory, the following definitions:

- **Multiple-cell upset (MCU)**: A single event that induces several cell upsets in an integrated circuit to fail at one time. The struck cells are adjacent (contrary to the corresponding error bits that are not always adjacent).
- **Multiple-bit upset (MBU)**: A multiple-cell upset in which two or more error bits occur in the same word data (an MBU cannot be corrected by a simple single-bit error-code correction).
- **Single-event functional interrupt (SEFI)**: A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single event burnout (SEB). Some SEFIs require power cycling the device. This is the case for example for new

types of complex ICs, such as microprocessors, DDR3 and NAND Flash memories. Note that a SEFI is often associated with an upset in a control bit or register.

- **Hard error**: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events). The error is “hard” because the data is lost and the component or device no longer functions properly even after power reset and re-initialization. The generic term single-event hard error (SEHE) is also used in literature.
- **Linear energy transfer (LET) of a particle**: The energy lost by unit of length, which is expressed here in MeV cm²/mg (1 pC/µm ≈ 100 MeV cm²/mg in Silicon). The magnitude of the disturbance an incident particle causes primarily depends on the LET of that particle.

2.5 SEU mechanisms in memories (SBU, MCU)

DRAMs, but also SRAM cells and SRAM-based programmable logic devices are subjected to single event upset mechanisms. Unlike capacitor-based DRAMs, SRAMs are constructed of cross-coupled devices, for which the capacity of each cell is significantly less elevated. The possibility of occurrence of an upset is greater when the capacity of a cell is lower. Given that the supply voltage and the cell size are reduced with each technological generation, the capacity of SRAM cells continues to decrease, making the cell more vulnerable to more types of particles (i.e. particles with lower energy). A particle that strikes a sensitive region of a memory cell deposits a dense track of electron-hole pairs. If the collected charge at a particular sensitive circuit node exceeds the minimum charge that is needed to flip the value stored in the cell, a soft error occurs. An error due to a hit of a single particle is called a single event upset (SEU).

Fig. 4 illustrates the occurrence of a SEU in a standard single port SRAM cell composed of two CMOS inverters and two access transistors connecting the storage nodes to the bit lines. When the word line (WL) is low (access transistors in the off-state), the cell is holding its stored data using the back-to-back inverter configuration. If the particle strike causes a transient on one of the nodes, the disturbance can propagate forward through the CMOS inverter and induces a transient in the second node. The second node, in its turn, leads the first node towards a wrong value and consequently the two nodes will flip. Then, the memory cell will reverse its state and will store a false value [36]; there is no mechanism to restore its state other than explicitly rewriting the state via the two complementary bit lines. In this sense the SEU is a reversible phenomenon that does not lead to the destruction of the cell.

Note that SEUs can also occur when the particle strikes the bit line [36-37]. During the read operation, a bit line is discharged through a small current from a memory cell. The bit of information is read as “0” or “1” based on the voltage differential developed on the bit line during the access period of the memory cell. This voltage differential can be easily disturbed if a particle strikes close to a diode of an access transistor of any cell on this bit line.

The minimum amount of collected charge that results in a soft error is called the critical charge (Q_{crit}) of the SRAM cell. The collected charge in the junction depends on many factors: the gate length, the substrate structure, the bias of the circuit nodes, the doping level in the device and the characteristics of the incident particle (such as energy, path and charge). The minimum amount of charge required to disturb a memory element is called critical charge and depends on the node capacity and the supply voltage. In SRAM cells and flip-flops, the critical charge depends also on the strength of the feedback transistors. The emergence of a soft error in the circuit following the impact of a particle depends on the energy of the incident particle, the geometry of the impact, and the design of the logic circuit. For simple isolated junctions (such as DRAM cells in storage mode), the impact of a particle induces a soft error if the collected charge is higher than the critical charge. In SRAM and logic circuits with active feedback, a soft error occurs only when the collected charge is greater than the critical charge by a certain factor that depends on the compensation

current from the feedback. Generally, a higher critical charge means less soft errors, but at the same time, a higher critical charge also means higher power dissipation and a slower logic gate.

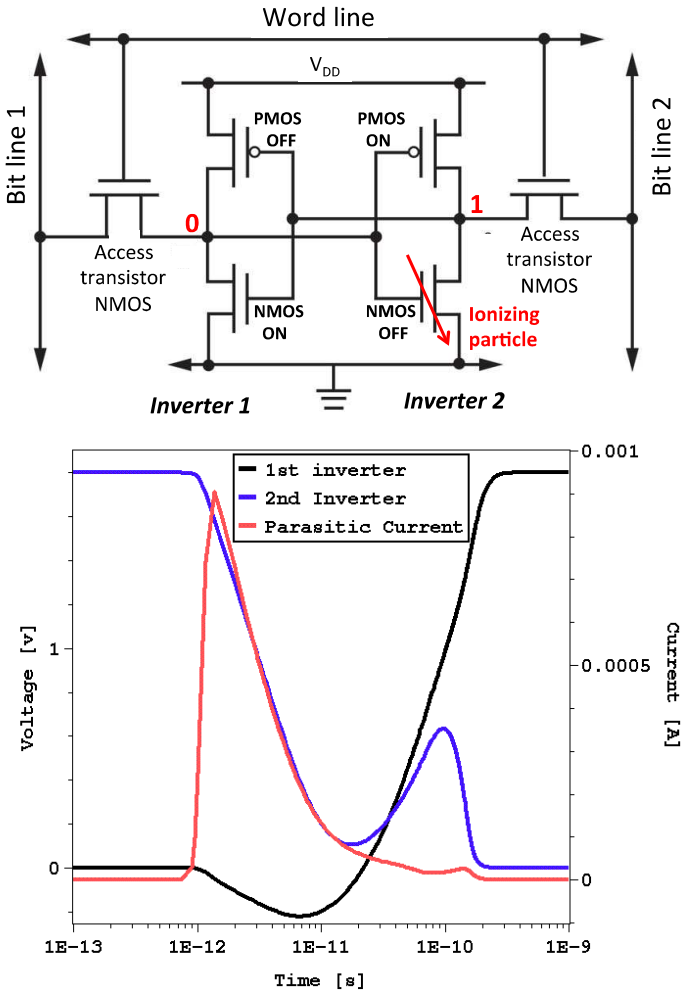


Figure 4: (top) Schematic circuit for an SRAM cell and (bottom) illustration of the transient currents induced by a ionizing particle striking the NMOS transistor (OFF-State) of the second inverter. Data courtesy of P. Roche (STMicroelectronics).

The rate at which soft errors occur is called the Soft Error Rate (SER) and is typically expressed in terms of Failures In Time (FIT) (the number of failures per 10^9 hours of operation). A practical equation used during accelerated or real-time test for example is $SER = \frac{N_r}{AF \times \Sigma_r} \times 10^9$ *(FIT / MBit)* where N_r is the number of bit flips observed at time T_r, Σ_r is the number of MBit×h cumulated at time T_r and AF is the acceleration factor (i.e. the amplification factor of the particle flux) with respect to a given reference (New-York City for example for the atmospheric neutron flux).

Another important SEU mechanism in memories is related to multiple cell upsets (MCU) and multiple bit upsets (MBU). Their increasing importance for state-of-the-art memories comes from the fact that the reduction of circuit feature sizes increases the probability that a single particle strike simultaneously affects several adjacent cells, depending of the particle track structure and characteristic dimensions. The topological shape of MCUs detected in a given memory plan results from a complex combination of the memory layout (alternative structure of vertical p-wells and n-wells) with the test pattern considered to fill the memory plan and with the particle-induced perturbation. Most modern memories now interleave logical bits from different words so that bits from the same logical word are never physically adjacent in the memory plan, strongly reducing the occurrence of MBUs. This issue will be discussed and illustrated in section IV for advanced SRAMs.

2.6 SEE mechanisms in digital circuits

With the continuous decreasing of the CMOS feature size, it is well established that single event transients (SETs) become significant error mechanism and are of great concern for digital circuit designers. CMOS scaling is accompanied by higher operating frequencies, lower supply voltages, and lower noise margins which render the sensitivity of circuits SET increasingly higher [12], [38]–[47].

Digital single-event transients (DSETs) constitute a temporary voltage or current transient generated by the collection of charge deposited by an energetic particle [48]. Even if this transient does not induce an SEU in the struck circuit, it can propagate through the subsequent circuits and may be stored as incorrect data when it reaches a latch or a memory element [15]. Unlike an SRAM cell (where an SEU occurs as a "persistent" error when a SET with sufficient charge impacts a critical node), in a combinational logic node an SET with sufficient charge may become manifested as a "persistent" error only if it propagates through the circuit and is latched into a static cell [46]. DSETs must fill a certain number of conditions in order to induce an error within a memory element [12], [49]:

(1) The ion strike must produce a transient able to propagate in the circuit.

(2) There must be an open logic path by which the DSET can propagate to reach a latch or a memory element.

(3) The DSET must have sufficient amplitude and duration to change the latch/memory state.

(4) In synchronous logic, the DSET must reach the latch during a clock pulse enabling the latch. Then the probability of capturing an SET increases with increasing clock frequency.

Digital circuits are constituted from sequential elements (e.g., latches, flip-flops, register cells) and combinational logic (e.g., NAND and NOR gates). The effects of single-event induced transients in these two types of circuits are succinctly described in the following.

Sequential logic. Typical sequential elements in the core logic are a latch [Fig. 5(a)], a domino cell [Fig. 5(b)] or a register file cell [Fig. 5(c)]. State changes can occur in core logic similarly to memory elements. In sequential logic (like in SRAM) the soft error rate has been found to be independent of the clock frequency of the circuit [50]. For example, the latch state can be flipped by the charge deposited by a particle strike on a circuit node regardless of the state of the clock signal.

Flip-flop circuits (Fig. 6) are other typical sequential logic circuits. With technology scaling, flip-flops have become more susceptible to soft errors, mainly due to the decrease in supply voltage and in their node capacitances. The simplified schematics of Fig. 6 shows that flip-flops circuits are similar to SRAM cells, as both apply feedback loops of cross-coupled inverter-pairs. As noted in part II, the soft error sensitivity of this class of circuits is determined by the critical charge (Q_{crit}) and the collection efficiency (Q_S). In an SRAM cell Q_{crit} is mainly the same for the two storage nodes because the cell is symmetrical. In flip-flops, the inverters are sized differently and have different fan-outs, which makes the flip-flop circuit asymmetric compared to the SRAM cell. Then, the individual storage nodes in a flip-flop have a different critical charge than in a SRAM and their SER sensitivity can vary with several orders of magnitude [51].

Combinational logic. Any node in combinational circuit can be impacted by an SEU and cause a voltage transient which can propagate through the combinational stages [Fig. 5(d)] and causes an error if latched by a sequential element, such as a memory cell. In combinational logic a certain number of transients will not be latched and even latched, some of these data will not be perceived as errors for the software operation. A transient error in a logic circuit might not be captured in a memory circuit because it could be masked by one of the following three phenomena [36], [53]:

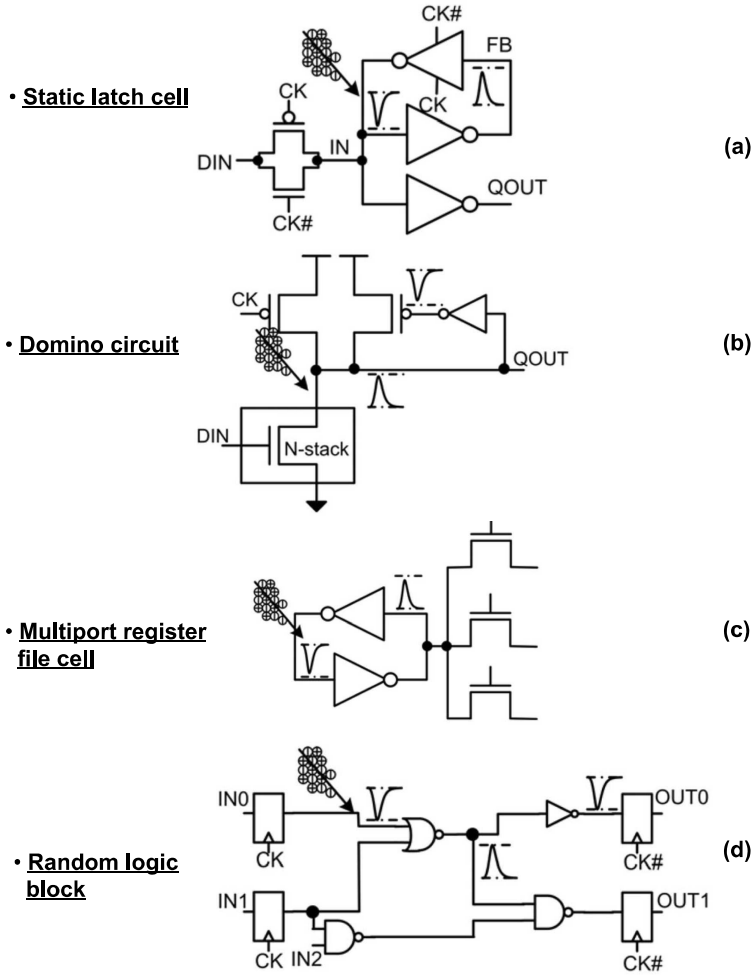


Figure 5: Illustration of typical sequential logic (latch, domino, register) and combinational circuits (random logic block). Adapted after Karnik et al. [36]. © 2004 Institute of Electrical and Electronics Engineers Inc.

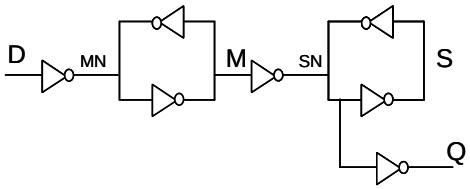


Figure 6: Simplified schematic of the flip-flop circuit. The sensitive nodes are labeled as MN, M, SN and S. After Roche et al. [52]. © 2005 Institute of Electrical and Electronics Engineers Inc.

(i) logical masking [53-54] occurs when a particle strikes a portion of the combinational logic that can not affect the output due to a subsequent gate whose result is completely determined by its other input values. For example, if the strike happens on an input to a NAND (NOR) gate [as illustrated in Fig. 40(a)], but one of the other inputs is in the controlling state [e.g., 0(1) for a NAND (NOR) gate], the strike will be completely masked and the output will be unchanged (i.e., the particle strike will not cause a soft error).

(ii) temporal masking (or latching-window masking) occurs when the pulse resulting from a particle strike reaches a latch, but not at the clock transition where the latch captures its input value [53]. This is explained in Fig. 40(b): when the transient propagates towards a sequential element [a latch in Fig. 40(b)], the disturbance on node DIN may be

outside the latching window [55]. Hence, the error will not be latched, and there will be no soft error.

(iii) electrical masking occurs for transients with bandwidths higher than the cutoff frequency of the CMOS circuit. These transients will be then attenuated [56]. The pulse amplitude may reduce, the rise and fall times increase, and, eventually, the pulse may disappear [as shown in Fig. 40(c)]. On the other hand, since most logic gates are nonlinear circuits with substantial voltage gain, low-frequency pulses with sufficient initial amplitude will be amplified [36].

Due to these masking effects the soft error rate in combinational logic was found to be significantly lower than expected [36], [53], [55]. Additional to these masking mechanisms, two key-factors impact the soft error rate in combinational logic: the clock frequency and the SET pulse width [39]. With increasing clock frequency there are more latching clock edges to capture a pulse and then the error rate increases. The pulse width is a key parameter which determines both the distance the SET will travel through the combinational chain and the probability that the SET be latched in a memory element as wrong data [40]. The wider the SET pulse width, the greater probability it has of arriving on the latching edge of the clock. If the transient becomes longer than the time period of the clock, then every induced transient will be latched [45]. The SET pulse width and amplitude depend on both process and circuit parameters (substrate and/or epitaxial layer doping, circuit capacitance, etc.) [46].

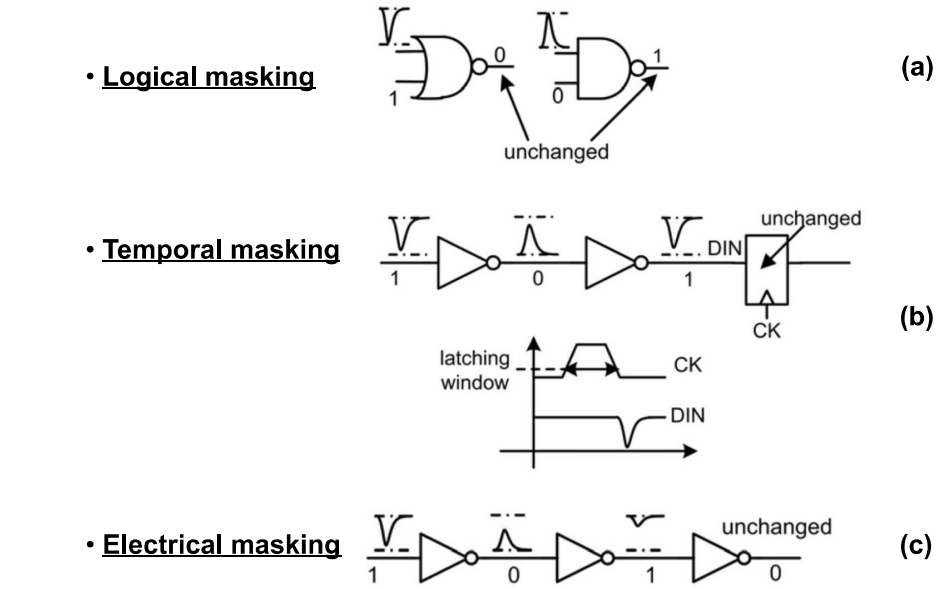


Figure 7: Illustration of the masking phenomena in combinational logic. Adapted after Karnik et al. [36]. © 2004 Institute of Electrical and Electronics Engineers Inc.

3 SEE modeling and simulation issues

Modeling and simulating the effects of ionizing radiation has long been used for better understanding the radiation effects on the operation of devices and circuits. In the last two decades, due to substantial progress in simulation codes and computer performances that reduce computation times, simulation reached an increased interest. Due to its predictive capability, simulation offers the possibility to reduce radiation experiments and to test hypothetical devices or conditions, which are not feasible (or not easily measurable) by experiments. Physically-based numerical simulation at device-level presently becomes an indispensable tool for the analysis of new phenomena specific to short-channel devices (non-stationary effects, quantum confinement, quantum transport), and for the study of radiation effects in new device architectures (such as multiple-gate, Silicon nanowire MOSFET), for which experimental investigation is still limited [57]. In these cases, numerical simulation is

an ideal investigation tool for providing physical insights and predicting the operation of future devices expected for the end of the roadmap. Last but not least, the understanding of the soft error mechanisms in such devices and the prediction of their occurrence under a given radiation environment are of fundamental importance for certain applications requiring a very high level of reliability and dependability [25].

The continuous reduction of the feature size in microelectronics requires increasingly complicated and time-consuming manufacturing processes. Then, a systematical experimental investigation of the radiation effects of new ultra-scaled devices or emerging devices with alternative architecture (such as multiple-gate or Silicon nanowire transistors) is difficult and expensive. Since computers are today considerably cheaper resources, simulation is becoming an indispensable tool for the device engineer, not only for the device optimization, but also for specific studies such as the device sensitivity when submitted to ionizing radiation. In addition, as the MOSFET dimensions are reduced in the nanometer scale, the device behavior becomes increasingly complicated while new physical phenomena specific to the ultra-short channels appear (such as quantum confinement, quasi-ballistic transport or parameter fluctuations). It becomes now mandatory to understand the mechanisms of these emerging phenomena and their impact on the device sensitivity to radiation. Then, the growing interest in modeling and simulation of single-event effects in microelectronic devices relies on unique capabilities, summarized below:

(i) Simulation provides useful insights into device operation since all internal physical quantities that cannot be measured on real devices are available as outputs in simulation. Several quantities in real devices are sometimes too small or too fast and cannot be measured.

(ii) “What if” studies, which are not feasible by experiment, can be performed in simulation [12].

(iii) The predictive capability of simulation studies makes possible the reduction of the radiation experiments [12].

(iv) Emerging phenomena appearing in ultra-scaled devices can be taken into account in simulation. The influence of these phenomena on the sensitivity to radiations of future device can be investigated in simulation studies.

(v) Simulation offers the possibility to test hypothetical devices which have not yet been manufactured.

3.1 Device-level modeling approach

Simulation of radiation effects at device-level aims to describe both the device (physical construction and electrical behavior) and its operation in radiative environment. Two methods can be used for this purpose, on one hand the device numerical simulation (TCAD) and on the other hand the use of compact models (which are later included in circuit-level SPICE-like simulations). In the following we describe these two simulation methods, highlighting the advantages and inconvenient of each approach.

Numerical modeling (TCAD). TCAD simulation at the device-level, also known as numerical modeling because it is based on the numerical solving of physics equations, is the most microscopic level, where it is possible to "see" the internal behavior of the device. This type of device simulation does not correspond to a circuit approach, but it is an essential step in the IC process development. Thus, numerical modeling aims to quantify the understanding of the underlying technology and abstract this knowledge for use in circuit design. TCAD numerical modeling consists of two distinct parts: the simulation of the manufacturing process and the simulation of the device electrical operation (device electrical simulator). The process simulator models the various stages of the device fabrication, such as ion implantation, deposition, etching, annealing and oxidation. The device electrical simulation models the electrical behavior of a device created by the simulation process taking into account its geometry, materials and doping profiles. For this, the device is

represented as a meshed structure where each node has specific associated properties such as the type of material, the dopant concentration, etc. The electrical simulator solves the main differential physical equations, such as the Poisson equation and the transport and continuity equations. Thus, for each node, the carrier concentration, the electric field, etc. can be calculated. To numerically solve the partial differential equations finite element discretization is performed on the considered mesh. The main inconvenient of this type of simulation is the computation time, which can be very important depending on the mesh size and the solved equations (drift-diffusion, hydrodynamic). But the significant advantage of numerical modeling is the ability to access internal quantities of the simulation (which cannot be measured) which substantially facilitate the fine understanding of the physical and electrical mechanisms taking place in the device.

Transport models used in the simulation of the effects of radiation on microelectronic devices include approaches Drift-Diffusion [58-59], hydrodynamic model [60-62] and Monte Carlo approach [63-65]. The most widely used model is Drift-Diffusion model, but recently the hydrodynamic model began to be used extensively in the simulation of advanced technologies in order to take into account the effects of non-stationary, and in the study of partially depleted SOI devices, where impact ionization is of great importance in the operation of the devices. The physical mechanism of impact ionization consists in the generation of electron-hole pairs in the device regions where a strong electric field exists (like in the vicinity of the drain regions). An electron with a sufficient energy in the conduction band yields its energy to an electron of the valence band. This last electron then jumps in the conduction band and leaves a hole in the valence band. It thus results a carrier multiplication in the device and the energy threshold necessary for the phenomenon release is roughly the semiconductor bandgap energy. In the case of MOSFET devices, the impact ionization phenomenon becomes important for device operation at high drain biases. The electrons generated by impact ionization go into the channel and amplify the drain current. The holes are pushed back towards the substrate and are then evacuated or not, depending on the type of device. In bulk MOSFETs they are collected by the substrate electrode and create a substrate current. In partially depleted SOI MOSFETs, the existence of the buried oxide prevents the hole evacuation by the substrate electrode; they generally accumulate in the neutral region (body without external contact) of the Silicon film, and increase the body potential leading to drain current kink phenomenon. Modeling approaches of impact ionization based on the only electric field (such as in the traditional "Drift-Diffusion" model) causes important quantitative and qualitative errors [66]; in particular an over-estimation of the impact ionization rate is observed even for long devices. An energy dependent advanced model is then mandatory for a more accurate modeling of the impact ionization phenomenon [67].

In commercial simulation codes [68-69], the effect of a particle strike is taken into account as an external generation source of carriers. The electron-hole pairs generation induced by the particle strike is included in the continuity equations via an additional generation rate. This radiation-induced generation rate can be connected to the parameters of irradiation, such as the particle LET (defined as energy lost by unit of length - dE/dl). The particle LET can be converted into an equivalent number of electron-hole pairs by unit of length using the mean energy necessary to create an electron-hole pair (E_{ehp}) [70]:

$$\frac{dN_{ehp}}{dl} = \frac{1}{E_{ehp}} \frac{dE}{dl}$$

Equation 1

where N_{ehp} is the number of electron-hole pairs created by the particle strike. By associating two functions describing the spatial and temporal distributions of the created electron-hole pairs, the number of electron-hole pairs is included in the continuity equations via the following radiation-induced generation rate:

$$G(w,l,t) = \frac{dN_{ehp}}{dl}(l) \cdot R(w) \cdot T(t)$$

Equation 2

where R(w) and T(t) are the functions of spatial and temporal distributions of the radiation induced pairs, respectively. Equation (2) assumes the following hypothesis: the spatial distribution function R(w) depends only on the distance traversed by the particle in the material and the generation of pairs along the ion path follows the same temporal distribution function in any point. Since function G must fill the condition:

$$\int_{w=0}^{\infty}\int_{\theta=0}^{2\pi}\int_{t=-\infty}^{\infty} G\,w\,dw\,d\theta\,dt = \frac{N_{ehp}}{dl}$$

Equation 3

functions R(w) and T(t) are submitted to the following normalization conditions:

$$2\pi\int_{w=0}^{\infty} R(w)\,w\,dw = 1$$

Equation 4

$$\int_{t=-\infty}^{\infty} T(t)\,dt = 1$$

Equation 5

The ion track models available in commercial simulation codes usually propose a Gaussian function for the temporal distribution function T(t):

$$T(t) = \frac{e^{-(\frac{t}{t_C})^2}}{t_C\sqrt{\pi}}$$

Equation 6

where t_C is the characteristic time of the Gaussian function which allows one to adjust the pulse duration. The spatial distribution function is usually modeled by an exponential function or by a Gaussian function:

$$R(w) = \frac{e^{-(\frac{w}{r_C})^2}}{\pi r_C^2}$$

Equation 7

where r_C is the characteristic radius of the Gaussian function used to adjust the ion track width.

The validity of this set of equations to model the track structure of a ionizing particle, in particular with respect to ultra-scaled devices and circuits, will be discussed in paragraph 4.2.1.

Analytic and compact model approach. The second approach for the device-level modeling is the use of analytical of compact models. Numerical modeling approach presented above is computer intensive because they involve detailed spatial and temporal solutions of coupled partial differential equations on three-dimensional meshes inside the device. Although this numerical modeling of the device is intended to be very accurate, it is not fast enough for high-level circuit simulators (eg. SPICE). Therefore, faster transistors models, developed to approximate measured terminal characteristic and oriented towards circuit parameters, are used for circuit design. These models are called compact or circuit models. Compact models are models that are simple enough to be integrated into circuit simulators and are sufficiently precise to make the simulation results useful for circuit designers. Compact models are generally based on analytical formulae that describe the static/dynamic electrical behavior of the elementary devices constituting the circuit. The compact is then the key element that allows to establish the link between the device (which is itself closely related to technology) and circuit design. In order to adapt to new nano-transistors architectures, these compact models must evolve to integrate always more physics without altering their flexibility, both in terms of computation time and ability to numerical convergence. Additional details concerning the circuit-level simulation using compact models will be given in the following paragraph.

3.2 Circuit-level modeling approaches

Three main modeling approaches are used for the simulation of single-event effects at circuit-level: circuit-level simulation, mixed-mode and 3-D simulation of full circuit. In the following, we briefly describe these different circuit-level modeling approaches.

Spice modeling and simulation. Circuit-level SEE simulation can be performed using standard simulation codes widespread in the IC industry for circuit design and optimization, such as the popular Berkeley SPICE, Silvaco SmartSPICE, Synopsys HPSICE, Orcad PSPICE, Mentor Graphics ELDO simulators, etc. Circuit simulators such as SPICE solve systems of equations that describe the behavior of electrical circuits (e.g. Kirchoff's laws …). Basic components of these simulation codes are compact models; as stated in the previous paragraph, these models describe the static/dynamic electrical behavior of the devices constituting the circuit. Advanced compact models provide high accuracy with minimum computational complexity. For simulating single-event effects at circuit level, the single-event induced transient is usually modeled as a current source connected at the struck node of the circuit [Fig. 8(a)]. This approach is adequate for many purposes, but presents some limitations. Firstly, it requires that satisfactory compact models already exist. But the use of compact models always introduces a certain numerical error (directly linked to the model accuracy), and models that are adequate for digital circuit simulation may be inadequate for other applications. Secondly, the accuracy of the transient current used as the input stimulus may considerably affect the circuit simulation precision. A typical example is the use of the current transient resulting from the device-level simulation of an unloaded device. In [71] the response of a memory cell to single-event is simulated at the circuit-level with Spice. The stimulus used at circuit level to reproduce the effect of the ionizing particle is a current pulse obtained by simulating at device level (2-D simulation with PISCES) the transient response of an unloaded device. In this case the circuit simulation inherits the inaccuracy of the improperly loaded device simulation [12].

Mixed-Mode approach. The limitations of compact models can be overcome by using physically-based device simulation to predict the response to ionizing radiation of the struck device. This approach is referred to as “mixed-mode” or “mixed-level” simulation, since the struck device is described by simulation in the device domain and the other devices by compact models. The two simulation domains are tied together by the boundary conditions at contacts, and the solution to both sets of equations is rolled into a single matrix solution [74-75]. Figure 8(b) shows the construction of a CMOS inverter chain in the frame of mixed-mode simulation. Only the struck NMOS transistor is modeled in the 3-D device domain. The current transient resulting from the ion strike on the struck device is directly computed by device domain simulation (there is no need for using an input stimulus which reproduces this current transient like in circuit-level simulation).

Mixed-mode capability is implemented in all major commercial device simulators [68-69], [76] and is generally used for the study of circuits with a reduced number of devices, as previously illustrated. Mixed-mode simulation provides several worthwhile advantages. No compact model needs to be specified for a numerical physically-based device. The approximation errors introduced by compact models or by input stimulus can be avoided. One can also access the internal device quantities (such as potential, electric field, carrier densities) within a physically-based device-level simulation at any point during the circuit simulation. In addition, mixed-mode technique can typically be used to simulate ionizing radiation impact in new devices (such as ultra-scaled multiple-gate and Silicon nanowire devices) and/or for taking into account emerging physical phenomena (e.g. quantum confinement or quasi-ballistic transport) for which compact models do not exist or are not yet satisfactory. In this case, all transistors contained in the circuit to simulate can be considered in the 3-D device domain.

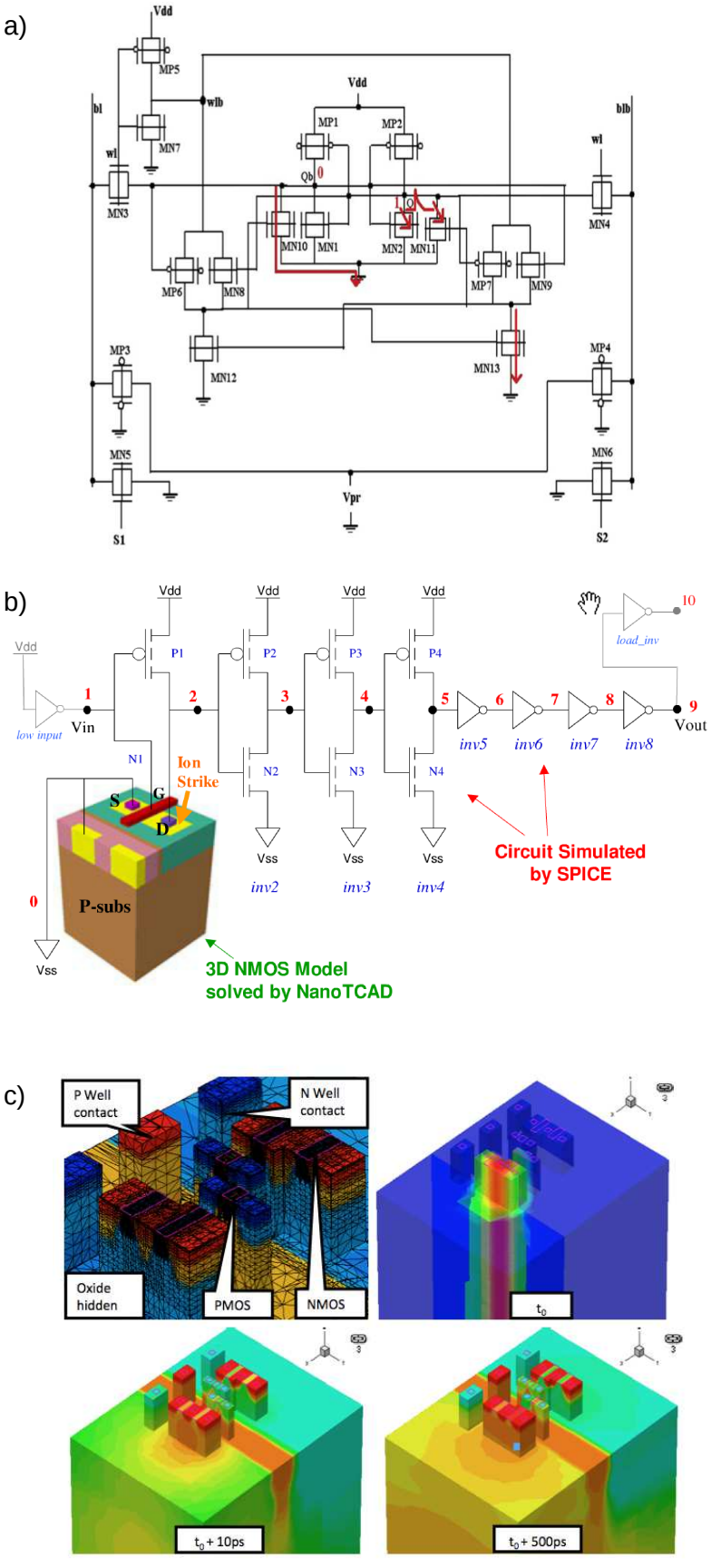


Figure 8: Illustration of the simulation approaches that can be used to investigate single-event effects at circuit level: (a) full SPICE simulation (DG-FinFET SRAM cell from [72]; (b) mixed-mode simulation (inverter chain, courtesy from CFD Research Corporation); (c) full 3-D numerical (full 3D single-port SRAM cell, courtesy from S. Uznanski [73].

The main inconvenient of the mixed-level simulation approach is the increased CPU time compared with a full circuit-level (SPICE) approach. In addition, mixed-mode simulation becomes not tractable for complex circuits. But, in the case of a SRAM cell for example, the 3-D mixed-mode simulations need significantly reduced computing times compared with the numerical simulation of the full cell in the 3-D device domain. Finally, it is important to note that 3-D mixed-level simulation is accurate for circuits only in the case where there are no coupling effects between the devices [12]. Since the spacing between devices will decrease with pushing the integration level, it is expected that coupling effects will become more important, and simulating the full circuit in the device domain may become mandatory [77-79].

Full numerical simulation in the 3-D device domain. The most accurate solution for studying SEE in circuits is to numerically model the entire impacted sub-circuit in the 3-D device domain. This was possible only recently (typically in the past decade), due to the enhancement of computer performances (CPU clock speed, memory resources) which reduced the computational time. Pioneering works of Roche et al. [77-78] and Dodd et al. [79] have demonstrated the capability of commercial codes to build and numerically simulate single-event-effects on complete 3-D SRAM cell. An example is shown in Fig. 8(c), with a full 3-D 6T SRAM cell [73]. Although the simulation time needed for simulation of the entire cell in the 3-D device domain was substantially reduced, it is still considerable compared with the time needed to simulate the same circuit with Spice and mixed-level approaches. The recent emergence of PC-based parallel machines (clusters) with hundreds of processors and important memory resource is certainly one very promising way to develop in the future such full 3-D simulations on large scale circuits or, more reasonably, portions of circuits.

3.3 Monte Carlo simulation tools

Full Monte-Carlo-based physical simulations of the SER provide a very powerful way to bring much more detailed physics to bear on the process of error rate prediction than has heretofore been possible with models and analytical computations [80-81]. Schematically, Monte Carlo simulation codes solve the radiation problem in two main steps, the interaction of radiation with the device and the subsequent motion of charges, and resulting changes in nodal currents and/or voltages, within the device/circuit. The complete simulation chain is complex due to its multi-scale and multi-physics character. Several code developments have been reported in the literature in the domain of single event effects. Here, we briefly mention a few works to illustrate these Monte Carlo approaches.

MRED:

The Monte- Carlo Radiative Energy Deposition (MRED) software developed at Vanderbilt is a framework for treating single event effects in integrated circuits in which the component tool describing radiation interactions and transport in matter is a built- in, Monte Carlo, binary-collision code. Figure 9 shows a block diagram of the core constituents of MRED. The basic philosophy is to be comprehensive in the treatment of all forms of radiation interacting with materials and to provide interfaces for smooth operation with related programs that handle other parts of the problem such as the transport of radiation-induced charge or the analysis of circuit effects of radiation-induced charge. As a system of software systems, probably the most important single design decision is the nature of the linguistic interaction between various independent constituents [80]. In MRED, Python is the chosen language for this interaction. For upset rate predictions, particle transport and energy deposition uses the Geant4 physics and a device geometrical model that includes the FEOL and BEOL structures. The use of Geant4 libraries allows modeling the spatial and temporal distribution of charge that is generated by a particle. Then, the energy deposition is tracked in the sensitive volumes, modeled as a set of Rectangular Parallelpiped (RPP) boxes.

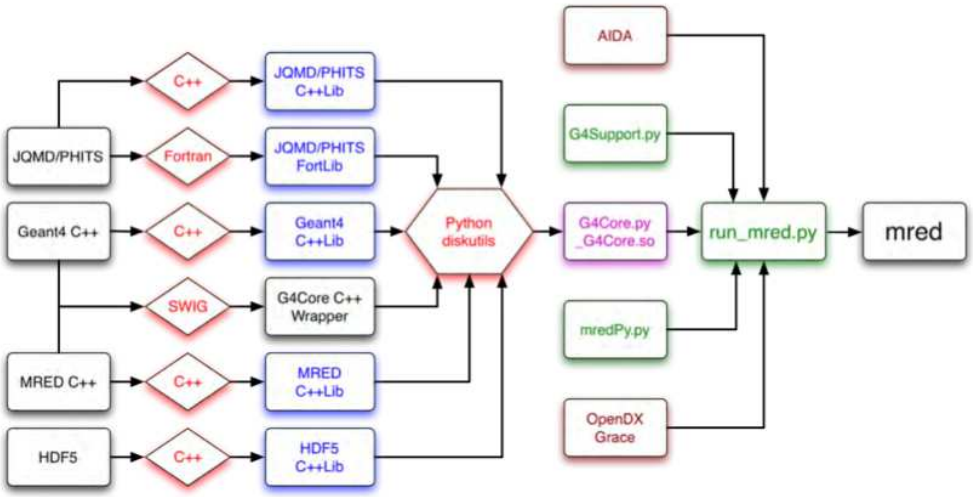


Figure 9: Architecture of the Geant4 application MRED, showing both the Geant4 core and other components. The actual program "mred" is a unix shell script that invokes the Python executable run_mred.py. The run_mred.py script loads several Python modules including G4Core.py, which contains most of the computing machinery. After Weller et al. [80].

SEMM-2:

The Soft-Error Monte-Carlo Model 2 (SEMM) approach developed at IBM is described in details in [82]. SEMM-2 is built from a number of independent modules, as illustrated in Fig. 10 (left). Each module has a distinct set of functions, and each generates output data for use by another. The modules are structured in such a way that they are only weakly linked with one another. Consequently, the addition of new modules and the implementation of new physics models into SEMM-2 is relatively straightforward.

SEMM-2 is intended to take into account the particle transport in the complex geometries and Back-End-Of-Line (BEOL) material compositions. Moreover, the different environment models have been developed to account for alpha particles, ion beam experiments, cosmic rays and other sources (Fig. 10 right). Similarly to Vanderbilt University's approach, SEMM geometry uses the sensitive volume approach and the upset occurrence is verified by critical charge criterion extracted from circuit simulations or experimental tests.

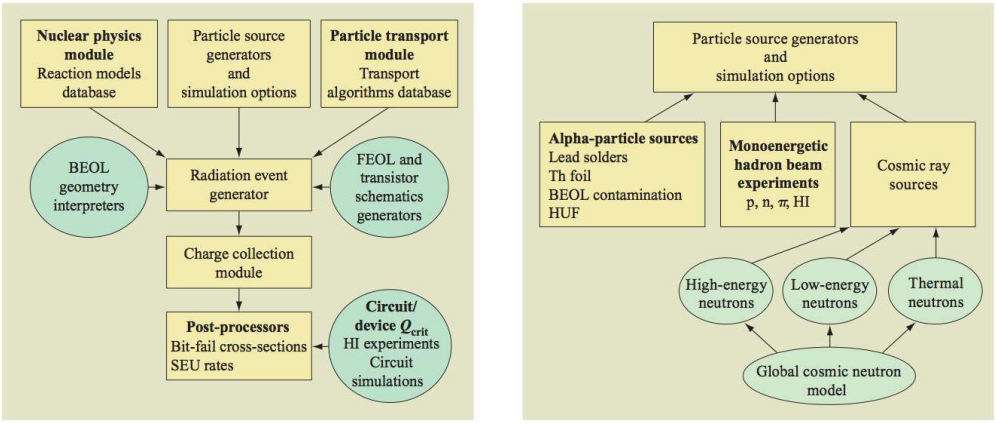


Figure 10: Left: Architecture and building blocks of SEMM-2. Right: Available simulation options in SEMM-2. After Tang et al. [82].

ORACLE:

Wrobel et al. from University of Monptellier II developed a tool called MC-ORACLE [83]. Previous versions developed in the same group were called PHISco (Prediction of Heavy Ion Sensitivity code) and MCDASIE (Monte Carlo De- tailed Analysis of

Secondary Ions Effects). Figure 11 shows a simplified flowchart for the code. ORACLE is based on the common empirical soft error criterion for a critical charge deposited in a parallelepiped sensitive volume. The code is able to deal with complex structures composed of various materials. The input parameters are the structure dimensions, the structure materials, the critical energy, and the sensitive volume dimensions (RPP criterion). The code can be applied to not just one type of particle, but to space ions and protons, atmospheric neutrons, and natural alpha emitters. As main output, ORACLE provides single and multiple error cross sections as well as the soft error rate.

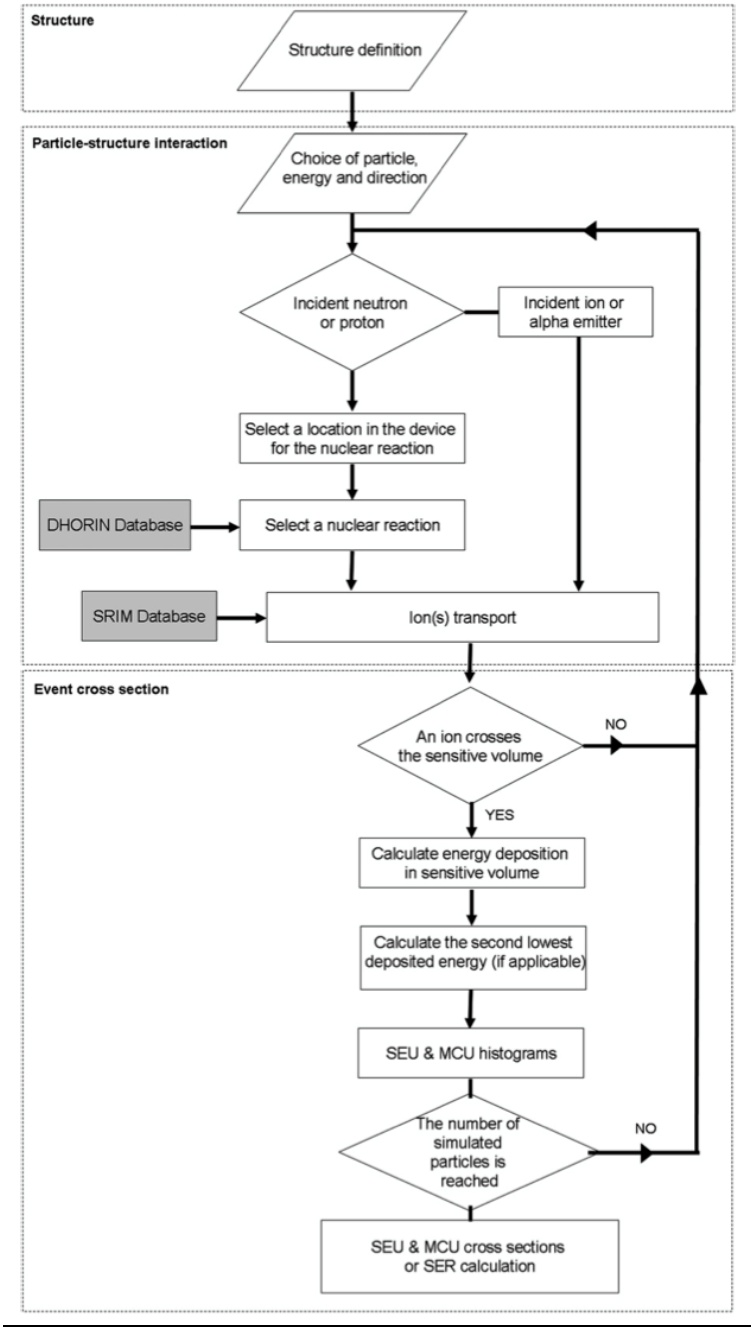


Figure 11: Simplified flowchart of MC-ORACLE. After Wrobel et al. [83].

TIARA-G4:

TIARA-G4 has been developed these last years conjointly at Aix-Marseille University (IM2NP laboratory) and at STMicroelectronics (Central R&D, Crolles). TIARA-G4 is a general-purpose Monte Carlo simulation code written in C++ and fully based on the Geant4 [84] toolkit for modeling the interaction of Geant4 particles (including

neutrons, protons, muons, alpha-particles and heavy ions) with various architectures of electronic circuits [85]. TIARA stands for Tool suite for rAdiation Raliability Assessment. The primary ambition of TIARA is to embed in a unique simulation platform the state-of-the-art knowledge and methodology of SER evaluation. The initial version of TIARA [86-87] was a standalone C++ native code dynamically linked with IC CAD flow through the coupling with a SPICE solver. The code has been developed such that the addition of new radiation environments, physical models or new circuit architecture should be quite simple. On one hand, this first version was able to treat the transport and energy deposition of charged particles (heavy ions and alpha particles) without the need for a nuclear code as Geant4; only SRIM [88] tables were used as input files to compute the transport of the particles in silicon and in a simplified BEOL structure reduced to a single layer. On the other hand, for neutrons, it used separate databases compiled using a specific Geant4 application to generate nuclear events in the simulation flow resulting from the interactions of incident neutrons with the circuit.

The new release of TIARA, used in this work, is called TIARA-G4, in reference to the fact that it is totally rewritten in C++ using Geant4 classes and libraries and compiled as a full Geant4 application. Nuclear events are no longer provided from databases but are directly generated in the flow of the simulation code by Geant4. This allows us to consider now all the complexity of the circuit in terms of materials, doping and 3D geometry, using the Virtual Geometry Model (VGM [89]) factory and interface with both Geant4 for calculation and Root [90] for visualization. In other words, the main improvement of TIARA-G4 with respect to the first version of the code comes precisely from this transformation of the code in a Geant4 application, allowing the use of Geant4 classes for the description of the circuit geometry and materials (now including the true BEOL structure) and the integration of the particle transport and tracking directly in the simulation flow, without the need of external databases or additional files. Figure 12 shows a schematics of the TIARA-G4 simulation description of the TIARA-G4 code and its different modules can be found in Ref. [85].

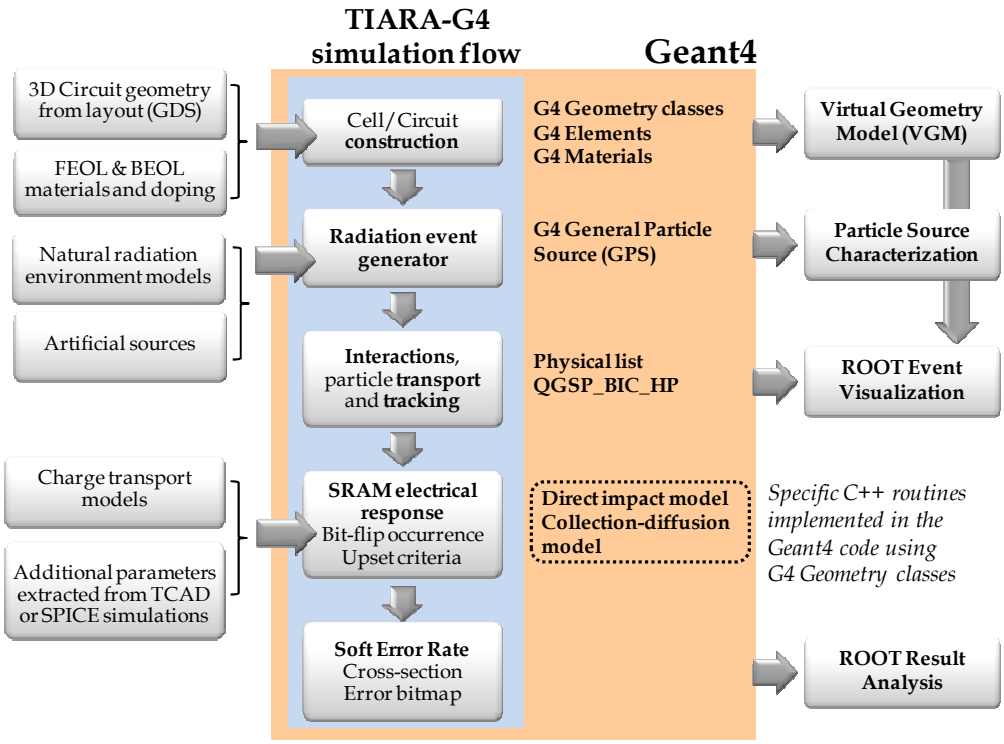


Figure 12: Schematics of the TIARA-G4 simulation flow showing the different code inputs and outputs and the links with Geant4 classes, libraries, models or external modules and visualization tools. After Autran el al. [85].

4 Evolving trends for emergent devices and circuits

4.1 The context: device and circuit roadmap

The continuous scaling of CMOS is driving information processing technology into a broadening spectrum of new applications. Many of these applications are enabled by performance gains and/or increased complexity realized by scaling [5]. The International Technology Roadmap for Semiconductors has emphasized in its early editions the “miniaturization” and its associated benefits in terms of performances, the traditional parameters in Moore’s Law [91]. This trend for increased performances will continue, while performance can always be traded against power depending on the individual application, sustained by the incorporation into devices of new materials, and the application of new transistor concepts. This direction for further progress is labeled “More Moore” (see Fig. 13).

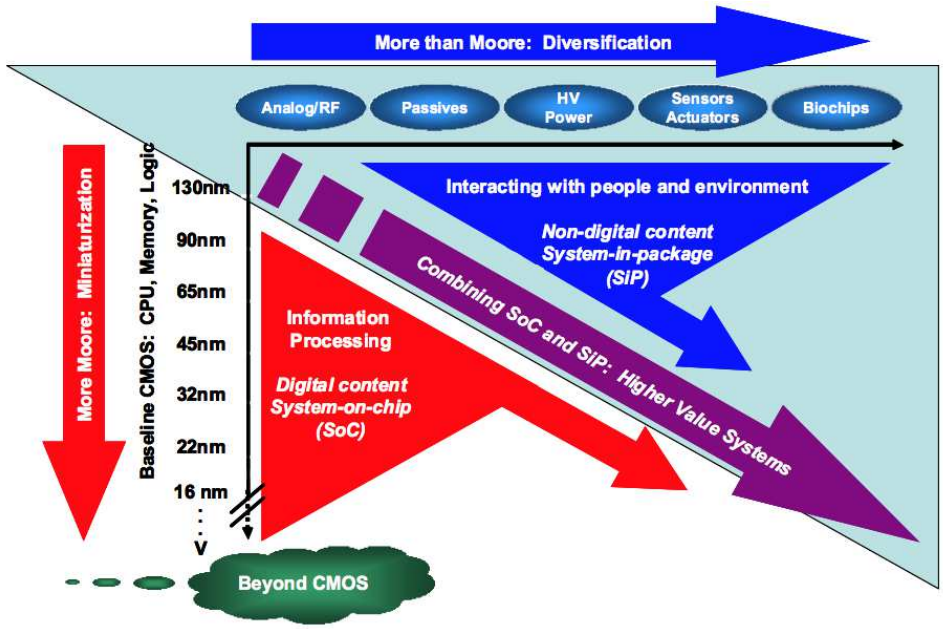


Figure 13: The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”). After Arden et al. [91].

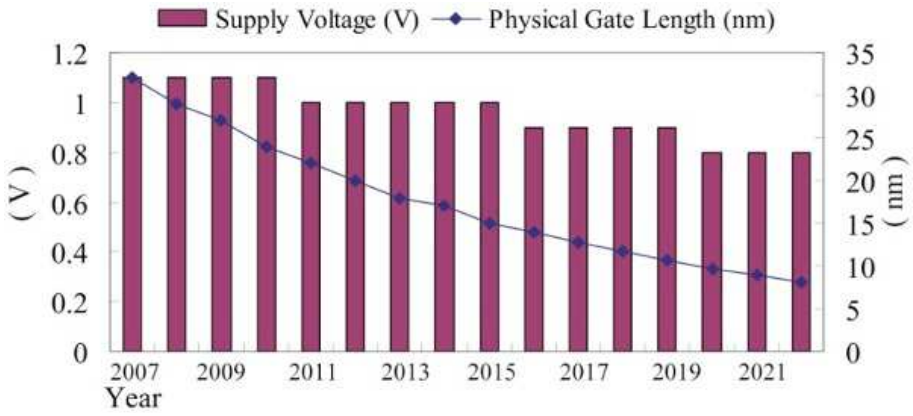


Figure 14: Trend for supply voltage and physical gate length predicted by the International Roadmap for Semiconductors (ITRS) [92].

Concerning precisely this "More Moore" trend, Figure15 illustrates the drastic reduction of both CMOS supply voltage and physical gate length as predicted by the International Roadmap for Semiconductors (ITRS) [92]. Also according to the ITRS roadmap in the next 10 years and as noted by Gasiot [93], the number of transistors per integrated system-on-chip (SoC) will be multiplied by 12. Soft errors in these SoC will thus grow accordingly if assuming a steady SER/bit. Soft errors are and therefore will continue to be a key reliability topic for most mass-customer applications (often responsible for the highest failure rate of all the reliability mechanisms). In addition, the metrics shown in Fig. 11, i.e. the dimensional scaling, the core voltage reduction, plus the increasing frequency of circuit operation, are three important facets of the famous Moore's Law that have direct (and not necessary concomitant) consequences of the evolution of the soft error rate with the integration. These aspects will be described and discussed in details in sections 4.2 and 4.3.

Another important facet of the Moore's Law is the transition from bulk to Silicon-on-Insulator architectures and from single-gate to multi-gate devices. The emergence of a large variety of new devices to continue to push the integration beyond the deca-nanometer range also directly impact the radiation reliability of circuits based on such device architectures. Section 4.4 will provide a survey of SEEs in ultra-thin fully-depleted SOI (UT-FDSOI) transistors and multiple-gate technologies.

Because dimensional scaling of CMOS eventually will approach fundamental limits, several new alternative information processing devices and micro-architectures for existing or new functions are being explored to sustain the historical integrated circuit scaling cadence and reduction of cost/function into future decades. The second trend is characterized by functional diversification of semiconductor-based devices. These non-digital functionalities do contribute to the miniaturization of electronic systems, although they do not necessarily scale at the same rate as the one that describes the development of digital functionality [91]. Consequently, in view of added functionality, this trend may be designated “More-than-Moore” (Fig. 13).

This "More than Moore" roadmap is necessarily more diverse for these devices, ranging from non-planar CMOS architectures to exotic new devices such as spintronics, carbon electronics or memristors. Since the exploration of these technologies has just started a couple years ago, published results concerning SEE effects are still too fragmented although few studies tend to show less sensitivity to radiation than current CMOS solutions. We will voluntary focus in section 4.5 on only a single aspect illustrating these "More than Moore" issues and sufficiently mature to give the first significant results at circuit level in a near-term perspective: the 3D integration.

4.2 Scaling effects in current technologies

While CMOS technologies continue to shrink in a "More Moore" perspective, several factors can directly impact their SEE susceptibility. We previously mentioned the reduction of the device dimensions, the increase of the operation frequency and the reduction of the critical charge/energy deposition necessary to cause a SEE. All these parameters not necessary influence in the same way the SER and certain are in competition, as explained in the following.

4.2.1 Feature size scaling

Geometrical scaling:

The reduction of device feature sizes combined with the increase of circuit integration (i.e. the number of transistor per unit area) has important implications for soft errors, as reported by Massengill et al. in [94]:

- the reduction of the per-bit cross-section presented to an incident ionizing particle;
- the reduction of the energy deposition volumes traversed by the particle;
- the increase of the particle region of influence in the circuit plan.

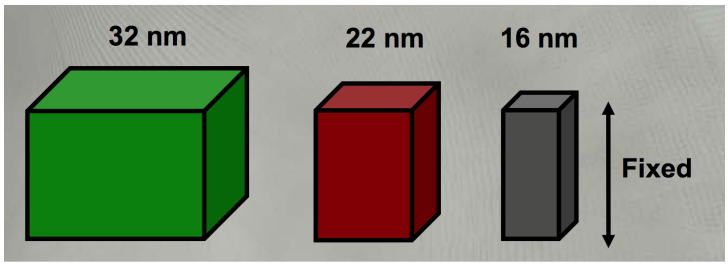


Figure 15: Illustration of the scaling of planar dimensions for three bulk technology nodes which is not been accompanied by like scaling of the vertical dimensions in the FEOL processing such as wells or epitaxial depths. After Sierawski et al. [95].

It should be noted that, for bulk technologies, the scaling of planar dimensions has not been accompanied by like scaling of the vertical dimensions in the FEOL processing such as wells or epitaxial depths. Consequently, the efficiency of energy transfer from an incident ionizing particle track to circuit nodes has scaled at a rate closer to the feature size squared rather than feature size cubed [94]. This important remark is schematically illustrated in Fig. 15 for current bulk technology nodes.

The recent migration from bulk to SOI technologies characterized by thin or ultra-thin top silicon layers totally isolated is an important geometrical factor that limits the single event deposition volumes; from a pure volumetric scaling point-of-view, the SER should decline if no other contrary phenomenon was involved in the soft error susceptibility of these new technologies.

Figure 16 illustrates the increase of the particle region of influence in circuit, which is one of the most spectacular observed effects in recent technologies. Because the impact of a single event is not punctual but has a certain radial extension (resulting in a radial charge distribution illustrated below), this spot of influence can intersect a more or less important portion of the circuit, depending on the technology node considered. In Fig. 16, the spot of influence of an alpha-particle intersects up to 6 memory cells in a 45 nm SRAM, whereas its impact was previously limited to a single cell for the 130 nm node. Such a pure geometrical effect is responsible in part (and in part only) of multiple cell upsets (MCU) observed in all recent technologies, typically below 130/90 nm technological nodes.

Ion-track spatial structure vs. device dimensions:

When pushing the integration, the influence domain of a single event not only concerns a part of the circuit but can have now an influence at device level since the characteristic radial dimension of a ion track structure has the same order of magnitude of the device feature size. Figure 17 (left) shows the comparison between two induced charge distributions in silicon by energetic heavy ions with the feature sizes of 0.25 µm and 50 nm SOI transistors. For the shortest device in particular, it is clear that a non-negligible part of the deposited charge is located outside the device. In other words, the deposited charge cannot be represented using a simple radial function, e.g. a simple cylindrical or Gaussian charge generation function with a uniform charge distribution and a constant LET along the ion path.

However, a real ion track structure has a more complex radial profile as a simple Gaussian function, as illustrated in Fig. 17 right). In addition, the track structure varies both in space and time when the particle passes through the matter. Immediately after the particle strike, the core of the track is characterized by the production of highly energetic primary electrons (called δelta rays). They generate further a very large density of electron-hole pairs in a very short time and a very small volume around the ion trajectory, referred as the ion track. These carriers are collected by both drift and diffusion mechanisms, and are also recombined by different mechanisms of direct recombination (radiative, Auger) in the very dense core track, which strongly reduces the peak carrier concentration. All these mechanisms modify the track distribution in time and space. As the particle travel through the matter, it loses energy and then the δ-rays become less energetic and the electron-hole pairs are generated closer to the ion path. Then, the incident particle generates characteristic cone-shaped charge plasma in the device [12].

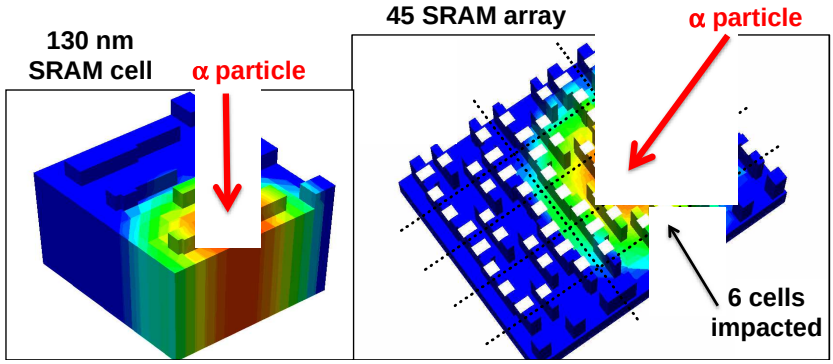


Figure 16: Illustration of the domain of influence of a single alpha-particle striking a SRAM in both 130 nm and 45 nm technologies. Only a single cell is impacted in 130nm whereas a cluster of 6 adjacent cells are impacted. TCAD screenshots courtesy of P. Roche [96].

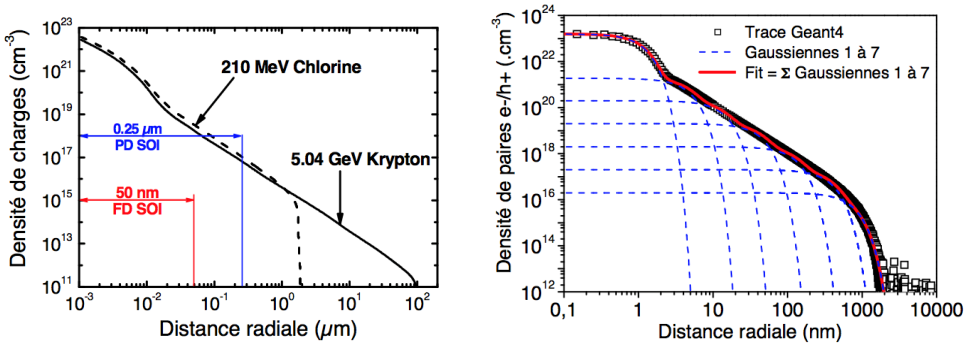


Figure 17: Left: Comparison of the radial charge distributions induced by 210 MeV chlorine and 5.04 GeV krypton ions in silicon with the feature size of 0.25 µm and 50 nm SOI transistors. Right: Reconstruction of a radial charge distribution (induced by the passage of an energetic ion in silicon) obtained using Geant4 with a sum of seven Gaussian functions [97]. © 2011 Institute of Electrical and Electronics Engineers Inc.

The real ion track structure has been calculated using various Monte-Carlo methods [98-100], including Geant4 code [101]. These simulations highlighted important differences between the track structure of low-energy and high-energy particles, in particular when the LET is the same (for details see [12], [102]).

To take into account these differences in device or circuit simulations, different practical approaches can be envisaged. The first one is to consider analytical models for ion track structure. Several models have been proposed in the literature and implemented in simulation codes. One of the most interesting models is the "non-uniform power law" track model, based on the Katz theory [103] and developed by Stapor [104]. Based on their theory, an analytical model was proposed by Waligorski [105] for ion tracks in water, and later adapted to silicon by Fageeha [106].

In this model, the ion track has a radial distribution of excess carriers expressed by a power law distribution and allows the charge density to vary along the track (i.e. the LET is not constant along the track) [107-108]. Other analytical models propose constant radius non-uniform track or Gaussian distribution non-uniform track. But, as mentioned in [109], all these models led to a radial distribution of energy deposition per unit volume proportional to the inverse square of the radial distance to the ion path. This dependence was then shown to be inaccurate, particularly for the track core region.

In [110], Rodbell et al. implemented into the IBM simulation code SEEM-2 a ion track model following a $1/r^2$ law (at large radii) and assuming a maximum radius of 1000 nm. They studied the impact of such a radial ion distribution on the magnitude of the SEU cross-sections for SOI latches in 32 and 45 nm technologies. This work shows that a Monte Carlo modeling with a realistic track structure is necessary to correctly reproduce experimental irradiation data, the classical line charge approximation (i.e. with no radius dependence) leading to a clear underestimation of the SEU cross-sections [110].

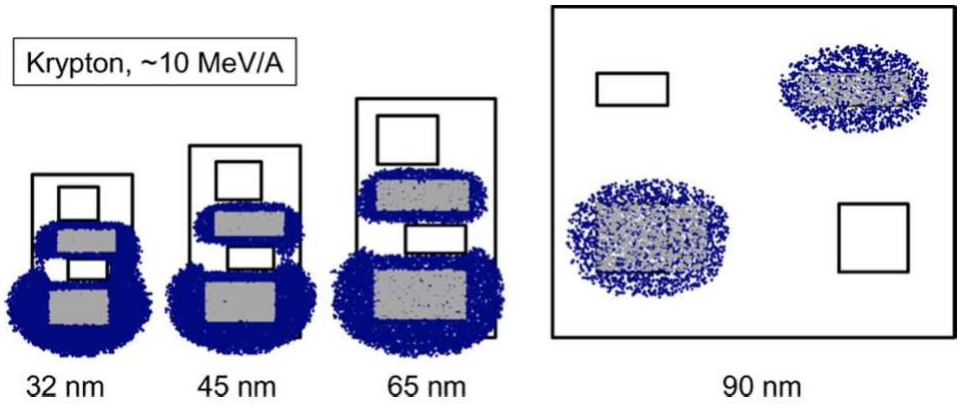


Figure 18: Cartographies of ion impacts leading to an SEU for a 10-MeV/A krypton ion incident in four SOI SRAM technology generations, either using the "punctual" (grey points) or "radial" (blue points) approach. After Raine et al. [109]. © 2011 Institute of Electrical and Electronics Engineers Inc.

To consider more realistic track structures, an interesting approach has been proposed by Raine et al. [97]: it consists in building a database of ion track structures obtained from Geant4 simulations and to fit a given track with multiple Gaussians [111]. This technique is illustrated in Fig. 17 (right). The resulting fitting coefficients are then used as input data in the Synopsys Sentaurus device simulator. TCAD simulation at device level can then be performed to evaluate the influence of the exact ion track structure on the transistor electrical operation.

The same authors have also recently investigated the influence of the radial dimension of the ion tracks at memory cell level using a Monte Carlo simulator. In this work, two ion track description have been compared: the "punctual" approach that considers an ion track as a series of punctual deposited charges (only taking into account the evolution of the LET with depth, with no radial dimension) and the new "radial" approach which proposes to use the realistic track structures obtained with Geant4. In this case, the distribution of deposited charge is discretized in both directions. Figure 18 shows the cartographies of ion impacts leading to an SEU for a 10 MeV/A krypton ion incident in four SOI SRAM technology nodes, either using the "punctual" or 'radial" approaches. Visually, the per-bit cross-section is larger for the "radial" approach as compared to the value obtained with the "punctual" description of the ion track. From this study, three major trends have been highlighted: 1) the ratio between the radial and the punctual SEU cross-sections increases with decreasing energy per nucleon—as long as the track is wide enough; 2) for a given technological node and energy per nucleon, the ratio increases with the ion mass and LET; 3) for a given ion and energy, the ratio increases with the technology integration.

Carrier channeling in wells and electrical related effects:

The reduction of circuit feature sizes has resulted in the emergence of regions where carriers in excess, as generated by a single event, can be confined or more exactly channeled in a certain region of the circuit at FEOL level. This particularly concerns the narrow wells of a given semiconductor type implanted in a semiconductor region of opposed type (eg. an N-well in a P-type substrate or vice versa).

The energy deposition along the particle track and the resulting generation of carriers in excess in such a well structure creates a charge injection, thus transiently perturbing the electrostatic potential distribution in the well. Moreover, the propagation of this charge in excess along the well extension can have a sufficient magnitude to trig parasitic bipolar injection from source to drain regions of transistors implanted in the same well. This effect has been observed and simulated in SRAM memories in particular for technological nodes below 90 nm.

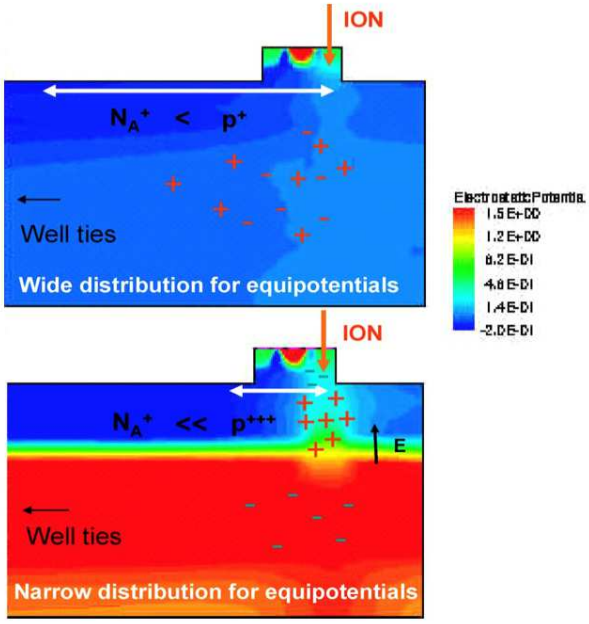


Figure 19: Electrostatic potential distribution around the ion track for a 65 nm SRAM memory cell away from well ties without triple-well (up) and with the triple-well (down). Without the TW, holes are deposited and diffuse in the P-well directly toward well taps. With the TW, high holes confinement is created (p+++) both by the narrow P-well transverse dimensions and the P-well/ TW junction, which quickly carries holes from the TW into the P-well. The positive charge gradient created between deposited holes (p+++) and well doping creates narrow distribution for the electrostatic potential. N_A^+ is the doping concentration in the P-well. After Giot et al. [112]. © 2008 Institute of Electrical and Electronics Engineers Inc.

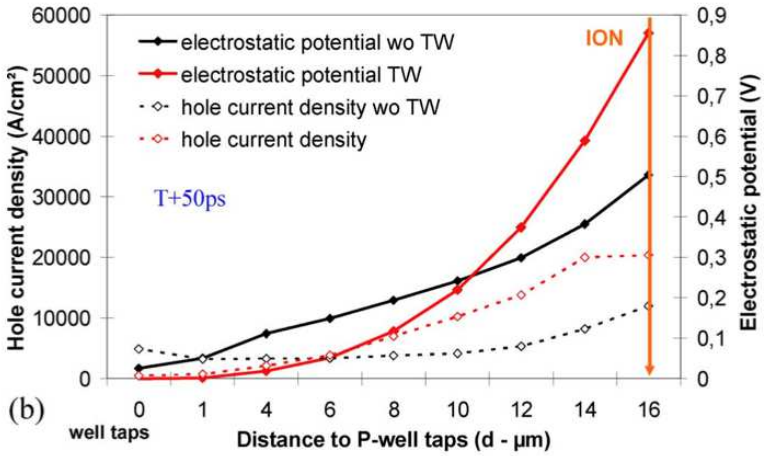


Figure 20: Full 3D TCAD simulation results for transient electrostatic potential and hole current density in the P-well area between ion track and well taps with and without the triple well option 50 ps after the ion impact. After Giot et al. [112]. © 2008 Institute of Electrical and Electronics Engineers Inc.

Figure 19 illustrates this phenomenon in the case of a SRAM circuit with and without a technological option called “triple well” (TW). This layer corresponds to either a N^+ or P^+ buried layer in respectively a P or N-doped substrate. On one hand, it has been used for years to decrease the Single-Event Latchup (SEL) sensitivity since the base resistance of the PNP parasitic bipolar is strongly reduced. TW makes accordingly the latchup thyristor more difficult to trigger on. On the other hand, the presence of TW electrically isolates the P-type wells related to the NMOS transistors of the SRAM cells, enhancing carrier channeling in such P-wells in case of single event

The narrow distribution for electrostatic potentials with the TW is explained by the intense hole current densities. This high current is created near the ion strike (Fig. 19) by the P-well triple well junction which rapidly carries holes into the P-well. This hole

current creates high positive charges gradient (high concentration of deposited holes p+++ near fixed charge in concentration in the P-well) in a small volume (narrower P-well transverse section with TW). This holes confinement within active areas (transistors) and TW induces high electric fields which explain the high variations of electrostatic potential observed around the ion track.

Figure 20 shows the simulated transient electrostatic potential and hole current density in the P-well area between ion track and well taps with and without the triple well option. At 50 ps and with TW, the electrostatic potential in the P-well around the struck bitcell is so high that the source still injects electrons into the P-well . The logic state of the drain allows it to recover rapidly a reverse biased junction and to collects high amount of electrons from the source. Without the TW, both the potential and current magnitudes have decreased. Thus there is no longer electrons injection from the source into the P-well.

Another example related to a more recent technology (40 nm SRAM) is illustrated in Figure 21. This figure shows the physical bitmaps of different MCUs detected during a real-time experiment conducted in altitude on the ASTEP platform. These large MCU events (≥ 10) correspond to high-density SRAM with a 25% reduced cell area with respect to the standard 40 nm node. This demonstrates the increase of the MCU sensitivity when increasing the technological integration and thus when reducing the memory cell area. The topological shape of the MCUs detected can be explained by the combination of the SRAM layout (alternative structure of vertical p-wells and n-wells) with the checkerboard pattern used to fill the memory plan. This is the reason why one can observe, for example, numerous horizontal pairs of adjacent cells (impact on the sensitive N-MOS drain of two adjacent cells, these two drains being located in the same vertical p-well) vertically aligned and a systematic alternating of sensitive and not sensitive horizontal rows (effect of the physical checkerboard). For all events characterized by a large multiplicity (≥10), it is clear that MCUs are preferentially in columns, due to the mechanisms of charge diffusion and channeling that propagate the perturbation (and consequently trig bipolar amplification) into the well directly impacted by the ionizing particle at the origin of the observed MCU.

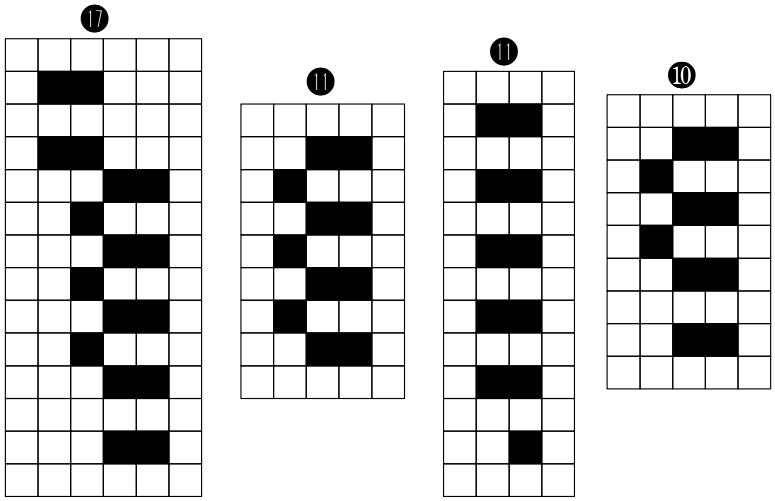


Figure 21: Physical bitmaps of the different MCUs detected for 40 nm single-port SRAM during a real-time experiment conducted in altitude on the ASTEP platform. Circle negative numbers indicate the event multiplicity. After Autran et al. [113]. © 2012 Institute of Electrical and Electronics Engineers Inc.

Variability and SEE:

Variability is an important challenge for current and future CMOS technologies, which increases as devices dimensions are scaled down. Two main sources of variability can be distinguished: global and local sources. As mentioned in [114], global variability sources correspond to all the process steps inducing a spread at transistor level such as threshold voltage and saturation current. Usual main variability sources are geometrical one, like physical gate length, offset-spacers and spacers width. They

are systematic factors modulating transistor parameters inside a die, across a wafer and lots. On the other hand, local variability sources are related to random effects. In Si/SiO_2-based bulk technologies, well-known sources are random dopant fluctuation and line edge roughness. Those two mechanisms degrade matching factor of transistors, which is fundamental for both SRAM functionality at low voltage and analog blocks performance as current mirrors. The recent introduction of high-k dielectric/metal gate stacks brings a new local variability as work-function modulation.

Both global and local variability sources can have a direct impact on the SER of circuits via the variations of device geometry or electrical characteristics resulting in variations of the critical charge for memories in particular. Two recent works illustrate such variability effects in SRAMs. In the first example [115], the impact of process-induced variability on the SRAM critical (Q_{crit}) charge has been studied from an analytical formulation of Q_{crit} derived for nanometric SRAM (see paragraph 4.2.2). Figure 22(a) shows the effects of threshold voltage (V_{TH}) variations of the driver and load transistors on Q_{crit}. The variations of Q_{crit} with slow and fast process corners (±6% V_{TH} for p-MOS, (±3% V_{TH} for n-MOS) are also reported in Fig. 22(b). Calculated values of Q_{crit} are found in excellent agreement with SPICE simulation.

Such critical charge variations inevitably induce soft error rate variations, as illustrated in the second example recently published by Gasiot et al. [93]. In this work, the variability encountered in a commercial 90 nm CMOS process has been characterized by studying die-to-die variation on a large population of dies from a single wafer.

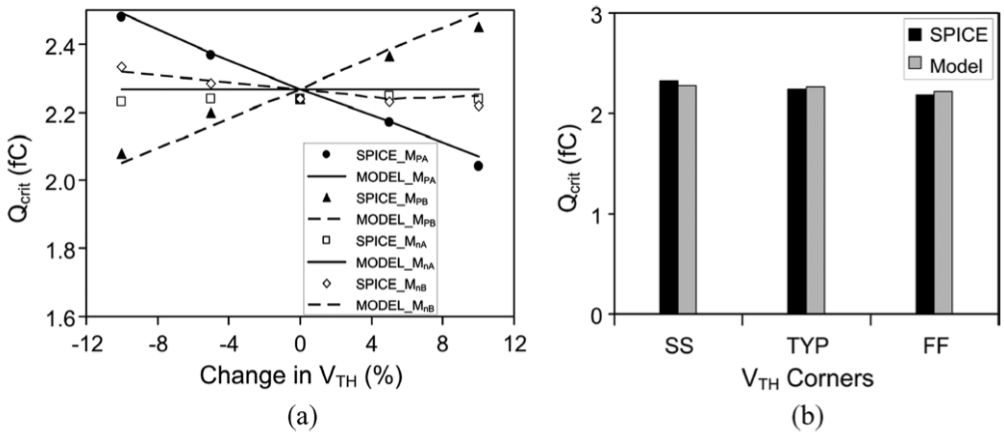


Figure 22: Critical charge (Q_{crit}) variations as a function of threshold voltage (V_{TH}) variations and V_{TH} corners as deduced from an analytical model for soft error critical charge of nanometric SRAMs. After Jahinuzzaman [115]. © 2009 Institute of Electrical and Electronics Engineers Inc.

The dies have been characterized with alpha particles and atmospheric neutrons and SER spread investigated as a function of their original position on the wafer. Moreover, experimental SER spread has been compared to circuit simulations based on manufacturer's Process Design Kit that takes into account by default parameters spread due to process variability. SER distributions have then been derived from the critical charge statistical distribution computed using an analytical model calibrated with experimental data. Figure 23 shows the comparison between experimental and simulated distributions for neutron and alpha SER related to 60 instances of 90 nm SRAMs. The good agreement between the two sets of experimental and simulated data demonstrates the interest of the method to derivate SER variability from the critical charge statistical distribution determined from process variation estimators.

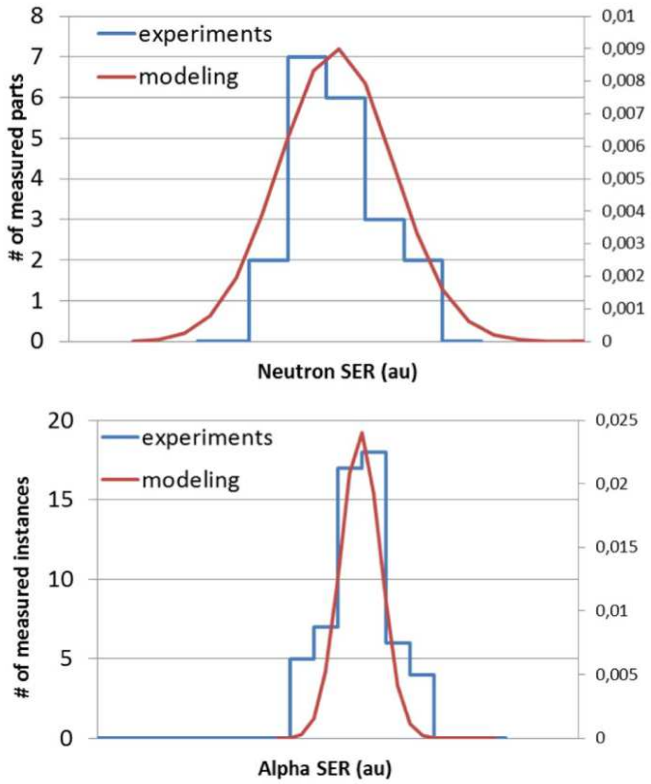


Figure 23: blue curves: experimental neutron and alpha SER of 60 SRAM instances measured on the same wafer and sorted by intervals of 20 FIT/Mb for 90 nm SRAMs. Red curves: probability densities of both neutron and alpha SER obtained from critical charge distributions using an analytical model calibrated with experimental data. After Gasiot et al. [93]. © 2012 Institute of Electrical and Electronics Engineers Inc.

4.2.2 Critical charge

As introduced in 2.5, the concept of critical charge (Q_{crit}) is a first-order metric that has been introduced to quantify the susceptibility for a static memory to be upset from a logical state to the other. It corresponds to the minimum amount of electrical charge that can flip the data bit stored in a memory cell. Its relationship with the circuit soft-error rate (SER) is exponential, as illustrated by the analytical model developed by Hazucha and Svensson [116]:

$$SER = K \times A \times Fe \times xp\left(-Q_{crit}/Q_S\right) \qquad \text{Equation 8}$$

where K is a scaling factor, F is the particle flux ($cm^{-2} \times s^{-1}$), A is the area of the circuit sensitive to particle strikes (cm^2), Q_{crit} is the critical charge and Q_S is the charge collection efficiency of the device (same unit as Q_{crit}).

Two key parameters for SER are the critical charge (Q_{crit}) of the SRAM cell and the charge collection efficiency (Q_S) of the circuit. Q_S and Q_{crit} are determined by the process technology [116], whereas Q_{crit} also depends on characteristics of the circuit, particularly the supply voltage and the effective capacitance of the drain nodes. Q_{crit} and Q_S are essentially independent, but both decrease with decreasing feature size. Eq. (8) highlights that changes in the ratio $-Q_{crit}/Q_S$ will have a very large impact on the resulting SER. The SER is also proportional to the area of the sensitive region of the device, and therefore it decreases proportionally to the square of the device size.

Different analytical/semi-analytical modelscan be used for estimatingQ_{crit} value in complement to full SPICE or TCAD approaches. We summarize in the following the brief review by Jahinuzzaman [115]. At first-order, $Q_{crit}$is simply modeled as a sum of capacitance and conduction components:

$$Q_{crit} = C_N V_{DD} + I_{DP} T_F \qquad \text{Equation 9}$$

where $C_N$is the equivalent capacitance of the struck node, V_{DD} is the supply voltage, $I_{DP}$is the maximum current of the on-state PMOS transistor and T_F is the cell flipping time. While both capacitance and conductance components indeed contribute to this critical charge, the first term is generally overestimated because the flipping threshold of an inverter is less than V_{DD} (V_{DD}/2 for perfectly matched NMOS and PMOS). In addition, the conductance term only considers the peak value of the current, which is not realistic. A more correct way for estimating the critical charge has been proposed by Xu et al. [117]:

$$Q_{crit} = \int_0^{Vtrip} C_N dV + \eta I_P T_{pulse} \qquad \text{Equation 10}$$

where V_{trip} is the static tripping point of the SRAM cell, η is a correction factor, I_P is the driven current of the on-state PMOS transistor and $T_{pulse}$is the duration of the particle-induced current pulse. Equation (10) provides a better estimation of the capacitance component of Q_{crit}, particularly the effect of junction capacitance and the addition of backend MIM capacitor. However, this model fails to incorporate the dynamics of voltage transient at the struck node, the quantitative description of I_{pulse}, and the contributions of the different transistors that constitute the cell. As a result, the accuracy of Eq. (10) in estimating Q_{crit} is limited.

Improved analytical techniques with reduced discrepancies (≤ 10% and below) with respect to full SPICE simulations have been proposed these last years by Zhang *et al.* [118] and more recently by Jahinuzzaman et al. [115]. This last model takes into account the dynamic behavior of the cell and demonstrates a simple technique to decouple the nonlinearly coupled storage nodes. Decoupling of storage nodes enables solving associated current equations to determine the critical charge for a classically used double exponential pulse current. The critical charge model thus developed consists of both NMOS and PMOS transistor parameters. Critical charge values calculated by the model have been found in good agreement with SPICE simulations for a commercial 90-nm CMOS process with a maximum discrepancy of less than 5%.

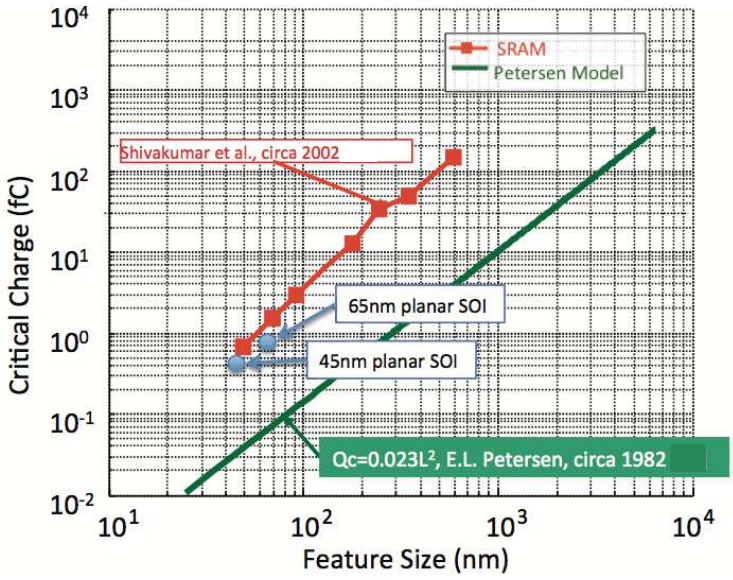


Figure 24: Critical charge scaling as a function of feature size. Data from Shivakumar et al. [53] are shown in red. The 1980's scaling model of Petersen [119] based on a second power dependence on feature size is shown in green. Also shown are recent data on planar SOI SRAM devices in blue. Plot courtesy of W. Seidler completed and adapted by Massengill et al. [94]. © 2012 Institute of Electrical and Electronics Engineers Inc.

Previous models, TCAD, mixed-mode or full SPICE simulations can be used to study the scaling of Q_{crit} as a function of transistor/circuit feature sizes. In a recent work, Massengill et al. [94] provides a compilation of Q_{crit} values for 6-T SRAMs as a function of feature size (Figure 24). As remarked by the authors, the early 1980's

prediction by Petersen of Q_{crit} scaling with feature size squared [119] has held remarkably accurate, even across decades of generational changes in substrates, lithography, and devices. Figure 24 shows that, for recent technologies, Q_{crit} values are now below the femtocoulomb, a value well below the amount of charge deposited by a single ionizing particle in silicon.

4.3 Increasing sensitivity to background radiation

4.3.1 Low-energy protons

The impact of low-energy protons on modern electronics is an important issue for both spatial and terrestrial applications. Low-energy protons are typically generated during scattering of high-energy protons or neutrons, and are primarily a concern in space radiation environments [120]. While shielding materials can easily absorb low energy protons, scattering of high-energy protons can yield significant fluxes of low-energy protons impacting electronics. Moreover, because secondary low-energy protons can be generated in nuclear spallation reactions of high-energy neutrons with silicon and other materials present in modern semiconductor devices, low-energy proton induced soft error upset rates (SER) also need to be accounted for in terrestrial radiation environments [121].

In the last years, several authors have reported on evidence of direct ionization from low-energy protons in SRAMs and latches [18], [111], [121-124]. As recalled by Seifert [120], low-energy proton energies in this context refer to proton energies that are at or below the lowest threshold energy for nuclear reactions of protons with silicon (Si), i.e., below the MeV [123]. The effect has been reported both in 65 nm bulk and 65 nm and 45 nm silicon-on-insulator (SOI) devices [18], [111], [121-123]. The authors showed that critical charges are well below 1 fC for the investigated devices and linear energy transfer (LET) values are sufficient to cause upsets via direct ionization.

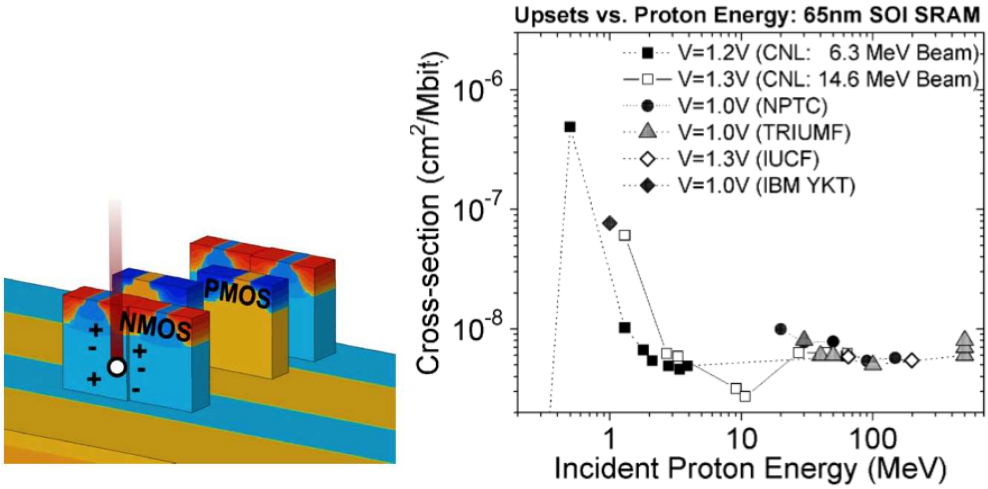


Figure 25: Left: Screenshot of a TCAD model of a 65 nm CMOS SRAM illustrating the passage of a low energy proton through the reverse-biased drain diffusion of a NMOS transistor (oxides have been omitted for illustration). The ionization core from the ion strike is also indicated. After Sierawski et al. [122]. Right: Experimental proton induced SEU data from 1 MeV to 500 MeV related to a 65 nm silicon-on-insulator (SOI) SRAM. After Heidel et al. [18]. © 2008-2011 Institute of Electrical and Electronics Engineers Inc.

This mechanism of direct ionization by low energy protons is well illustrated in Figure 25 (left) for a 65 nm CMOS SRAM. The TCAD investigations conducted by the authors in this study establish that the electronic stopping of protons, which have a peak LET near 0.5 MeV.cm^2/mg may induce upsets if the peak occurs near the sensitive device regions. Figure 25 (right) shows experimental results measured on a 65 nm silicon-on-insulator (SOI) SRAM subjected to beam of protons related to five SEU test facilities including: 1) the Tri-University Meson Facility (TRIUMF); 2) the Francis H. Burr Northeast Proton Therapy Center (NPTC); 3) the Indiana University Cyclotron Facility (IUCF); 4) the UC Davis Crocker Nuclear Lab (CNL); and 5) the

IBM Yorktown 3 MV Van de Graaff facility. The low energy proton SEU results are very different for this SRAM as compared with SRAMs fabricated in previous technology generations. Specifically, no upset threshold is observed as the proton energy is decreased down to 1 MeV; and a sharp rise in the upset cross-section is observed below 1 MeV. The increase below 1 MeV is clearly attributed to upsets caused by direct ionization from the low energy protons.

4.3.2 Atmospheric muons

As introduced in paragraph 2.2.1, atmospheric muons represent an important part of the natural radiation background at ground level. Muons belong to the Meson or “hard” component in the atmospheric cosmic ray cascades and are the products of the decay of charged pions (charged mesons π^+ and π^-) via the weak interaction. In spite of their short lifetime but because they are relativistic, these particles are easily able to penetrate the atmosphere; they constitute the most preponderant charged particles at sea level.

In more details, muons are charged particles with a unitary negative electric charge and a mass about 200 times the mass of an electron. The muon, denoted by μ^- and also called "negative muon", has a corresponding antiparticle of opposite charge and equal mass: the antimuon, often called "positive muon" (μ^+). Muons are unstable particles with a mean lifetime of 2.2 µs. Independently of any interaction with matter, they spontaneously decay into three particles:

$$\mu^- \rightarrow e^- + \overline{\upsilon}_e + \upsilon_\mu$$
$$\mu^+ \rightarrow e^+ + \upsilon_e + \overline{\upsilon}_\mu$$

Both negative and positive muons weakly interact with matter: they can travel large distances in matter, thus deeply penetrating into material circuits. Ziegler and Lanford have been the first authors to point out precisely how muons can interact with matter at relatively low incident primary energies [125]. They decompose the interaction into three primary processes:

1) **Muon direct ionization wake**. A charged muon loses its kinetic energy passing through semiconductor material by excitation of bound electrons and frees electron-hole pairs along its path as a result.

2) **Electromagnetic scattering** which induces energetic coulomb silicon nucleus recoil.

3) **Capture of the negative muons** by atomic nuclei when they are quasi stopped in matter. This complex capture mechanism releases recoiling heavy nuclei with a simultaneous emission of light particles (neutrons, protons, deuterons, α-particles, etc.). When negative muons stop in silicon, a particular but important case when investigating the effects of muons on electronics, about 35% in average decay into an electron and two neutrinos. The remaining 65% are captured [126]. If an intermediate state is assumed, the reaction is:

$$\mu^- + {}^{28}\mathrm{Si} \rightarrow {}^{28}\mathrm{Al}* + \nu_\mu + 100.5\ \mathrm{MeV}$$

Sobottka et al. [127] have measured the energy spectrum for charged particle emission resulting after muon capture in ^{28}Si following some modes of de-excitation of ^{28}Al recoiling nucleus:

$$\begin{aligned} {}^{28}\mathrm{Al}* &\rightarrow {}^{27}\mathrm{Al} + n\ (12.4\ \mathrm{MeV}) \\ &\rightarrow {}^{27}\mathrm{Mg} + p\ (14.2\ \mathrm{MeV}) \\ &\rightarrow {}^{24}\mathrm{Na} + \alpha\ (15.5\ \mathrm{MeV}) \\ &\rightarrow {}^{26}\mathrm{Mg} + d\ (18.4\ \mathrm{MeV}) \end{aligned}$$

where the energy listed with each final state is the ground-state energy with respect to the ^{28}Si ground state. According to the compilation of several works [127-132], among all the muons that are captured, 28% result in no particle

emission, 15% result in charged particle emission (~10% protons, 5% deuterons and <1% tritons or α-particles – in some cases, there may be several percents of alpha-particles), 67% result in neutron emission, with 10% emission of both charged particles and neutrons.

Until a recent period, the effect of muons on electronics has resulted in only a very small number of works. We can cite the pioneer work in the 80's of Ziegler and Lanford [125] and a few experimental characterization studies of memories (SRAM, DRAM) using artificial muon beams [20-22]. Recently, Sierawski et al. [23-24] conducted the first major work on the subject, combining measurements and numerical simulations on the effect of low energy (<3 MeV) and atmospheric positive muons on advanced technologies. They demonstrated and quantified the effects of muon direct ionization for different bulk SRAM of different technology nodes (65, 55, 45, and 40 nm). The data presented in Figure 26 show the probability of upset at nominal bias for four different SRAMs subjected to μ^+ irradiation using the M20B surface muon beam at TRIUMF.

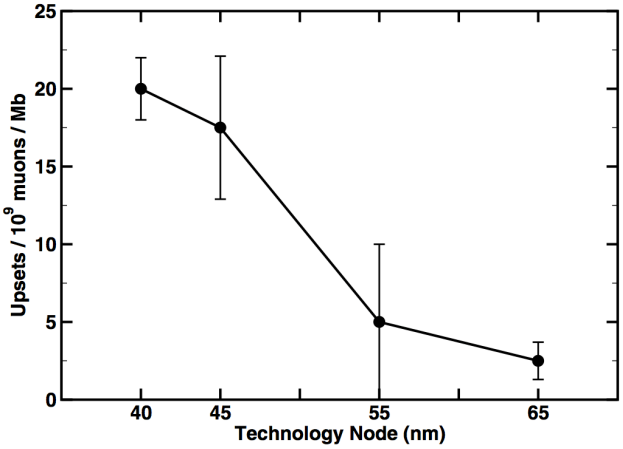


Figure 26: Experimental muon-induced single event upset probability for different SRAMs under test operated at nominal supply voltage and irradiated using a 21.6 MeV/c μ^+ beam. After Sierawski et al. [24]. © 2011 Institute of Electrical and Electronics Engineers Inc.

As stated by Sierawski et al. in their 2011 paper [24], these data show a clear increase in the SEU susceptibility and significance of energy deposition by muons for scaled technologies. To first order, the reduction of the device area results in a decrease in the number of particles passing through the cell and capable of producing an upset. This scaling would reduce the probability of a bit being in error in the beam. The increase in upset probability is therefore attributed to differences in the geometry of the charge collection, an increase in the fluence of energy deposition events exceeding the critical charge, or both. Further, in these experiments, the incident muons have a distribution of kinetic energies and therefore a distribution of stopping powers. As the technology node decreases, the charge required to upset a single memory cell decreases. The effect of this trend is an increase in the fraction of the distribution that is able to induce an upset. For the 40 nm SRAM, a larger portion of the 21.6 MeV/c beam exceeds the stopping power threshold as compared with the 65 nm SRAM. While the probability of upset is increasing for future devices, it cannot be ascertained from these data whether the trend is linearly or super-linearly increasing.

In complement to these experimental results, the authors performed a series of simulations with the Vanderbilt Monte Carlo Radiative Energy Deposition (MRED) code [80]. The estimated sea level error rates are shown in Figure 27 for 32, 22, and 16 nm representative sensitive volumes. Each curve increases for lower values of generated charge as one would expect a more sensitive device to have a higher error rate. Below the 32 nm technology node, the critical charge is decreased enough that this threshold now permits a significant rate of errors to occur. The results also indicate the potential for large variations in the error rate for 16 nm devices. The dramatic increase in the error rate for devices with a threshold below 0.2 fC suggest

that even minor design differences may have a large impact on the reliability of the memory.

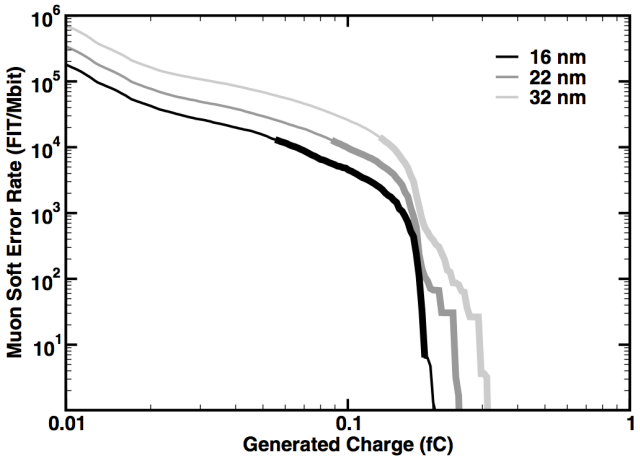


Figure 27: Estimated muon-induced event rate at NYC location versus generated charge curves for 32, 22, and 16 nm bulk CMOS representative sensitive volumes. Thick lines indicate the error rate for a technology node based on the range of critical charge values. After Sierawski et al. [24]. © 2011 Institute of Electrical and Electronics Engineers Inc.

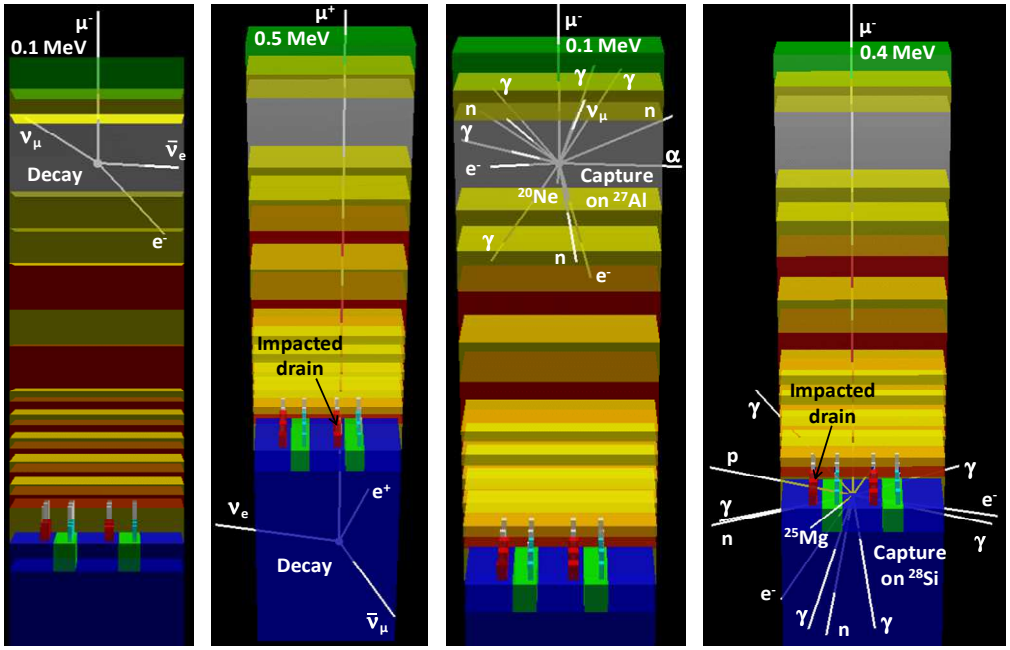


Figure 28: Visualization of four events illustrating the interactions of low energy negative and positive muons with a 65 nm SRAM structure. From left to right: μ- decay in the BEOL (Al layer), μ+ upsetting a drain by direct charge deposition though the structure followed by the muon decay in the substrate, μ- capture on an aluminum atom in the BEOL, μ- capture on a silicon atom in the active circuit region (Pwell) leading to a drain upset via a direct impact by a secondary particle (proton in this case). After Serre et al. [133]. © 2012 Institute of Electrical and Electronics Engineers Inc.

More recently, Serre et al. [133] studied the complementary effect of low energy (<1 MeV) *negative muons* on SRAM memories and evidence the importance of the *negative muon capture* mechanism as an additional mechanism of charge deposition for negative muons that can be stopped in silicon. Figure 28 illustrates different possible scenarios of negative and positive muon interactions with a 65 nm SRAM structure as simulated using the TIARA-G4 simulation code. Figure 28 (a) shows a negative muon decay in the top layers of the back-end-of-line (BEOL) structure; this cannot lead to an upset since the muon disintegrates in light particles not able to deposit any significant charge in silicon. Figure 28 (b) shows a similar event but occurring in the silicon substrate. In this case, the incoming positive muon traverses

the complete BEOL structure and, statistically, can cross a sensitive drain. If the charge deposited in the impacted drain is higher than the critical charge for this transistor type and for this technology, the corresponding memory cell is upset. Figures 28 (c) and (d) show two negative muon capture events occurring in the BEOL and in silicon, respectively. These events produce large secondary particle showers, containing one or more charged particles susceptible to reach the active silicon region and to induce an upset or even a multiple cell upset. Of course, the probability to induce an upset is maximum when the muon capture-induce shower is produced in the immediate vicinity of the sensitive drain layer, as illustrated in Figure 28(d). This case corresponds to a reduced energy interval for the incoming muons in so far as the penetration depth of the muons in the structure and then the capture location primarily depends on the muon kinetic energy.

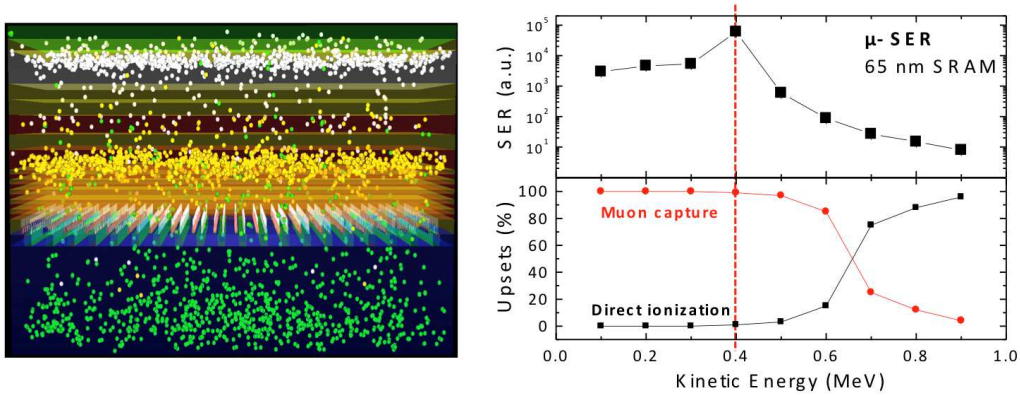


Figure 29: Visualization of four events illustrating the interactions of low energy negative and positive muons with a 65 nm SRAM structure. From left to right: μ- decay in the BEOL (Al layer), μ+ upsetting a drain by direct charge deposition though the structure followed by the muon decay in the substrate, μ- capture on an aluminum atom in the BEOL, μ- capture on a silicon atom in the active circuit region (Pwell) leading to a drain upset via a direct impact by a secondary particle (proton in this case). After Serre et al. [133]. © 2012 Institute of Electrical and Electronics Engineers Inc.

In order to illustrate this effect, Serre et al. plotted in Figure 29 (left) the distribution inside the SRAM structure of the vertex positions related to the negative muon capture reactions for three different values of the incident muon kinetic energy: 0.1, 0.3 MeV and 0.5 MeV. They clearly evidence in this figure such a dependency of the capture position (depth) with the muon kinetic energy. As a result, the soft error occurrence, and consequently the soft-error rate induced by negative muon irradiation presents a maximum when precisely muon captures occur at the depth of the layer containing sensitive drains (i.e. the active silicon region). This behavior is illustrated in Figure 29 (right) which also plots the percentage of cell upsets induced by muon capture reactions or directly by muon impacts on sensitive drain (i.e. direct charge deposition in drain volumes). When increasing the kinetic energy of primary particles, the fraction of upsets induced by muon capture rapidly decreases as soon captures occur deeper in silicon, below the active layer. In this case, upsets become mainly induced by direct charge deposition from incident muons.

In conclusion, these recent works clearly demonstrate the importance of low energy atmospheric muons as a new radiation constraint at ground-level for the most advanced CMOS technologies. Further works are necessary in the future to in-depth investigate in particular the exact proportion of positive and negative atmospheric muons that can significantly deposit charge in silicon with respect to not only the circuit architecture but also to the local environment (shielding) of the circuit, susceptible to profoundly impact the distribution of such low energy atmospheric muons below ~1 MeV. The current lack of both experimental and theoretical knowledge related to atmospheric muon distributions below 1 MeV should therefore represent a limitation to accurately estimate the impact of muons on electronics at ground level.

4.3.3 Low alpha material issue

The presence of alpha-particle emitter isotopes has been established in materials used in the chip package (such as solder balls or mold compounds) or directly integrated at wafer level (silicon, metal interconnects, more recently hafnium in new high-κ gate dielectrics or platinum in silicide layers [134]). With the downscaling of CMOS technologies, the sensitivity of ICs to alpha-particle emitter contamination is a crucial question because of the constant reduction of the supply voltage and node capacitance, as previously discussed. The direct consequence for current and future technologies will be clearly the need of lower alpha-emitting materials used at the different levels of the fabrication process. This includes not only packaging materials which generally represent the prime source of alpha contamination but also materials and alloys employed both at front-end (FEOL) and back-end of line (BEOL) levels. Because of their immediate proximity with circuit sensitive nodes, FEOL materials with extremely low levels of alpha contaminations can therefore represent a non-negligible source of soft errors.

As an illustration of the dangerousness of alpha-particle contamination at silicon level, Figure 30 shows the results of a cave real-time SER testing of 65 nm SRAMs conducted at the underground laboratory of Modane (LSM, France) during more than 3 years [135]. At the depth of the LSM, cosmic rays are totally screened and one can consider that soft errors are quasi exclusively due to the internal chip radioactivity, i.e. the alpha-particle emitters present in chip materials (ultra-low emissivity packages were used). The experiment involved 3,226 Mbits of standalone single-port memories and 90 bit flips were detected in approximately 24,000 hours of measurements. These results have been perfectly reproduced using a Monte Carlo SER simulation code and assuming 0.1 ppb of ^{238}U contamination in the silicon bulk of the circuits, demonstrating that a low alpha material (in this case the silicon wafers) can therefore be responsible of detectable soft errors.

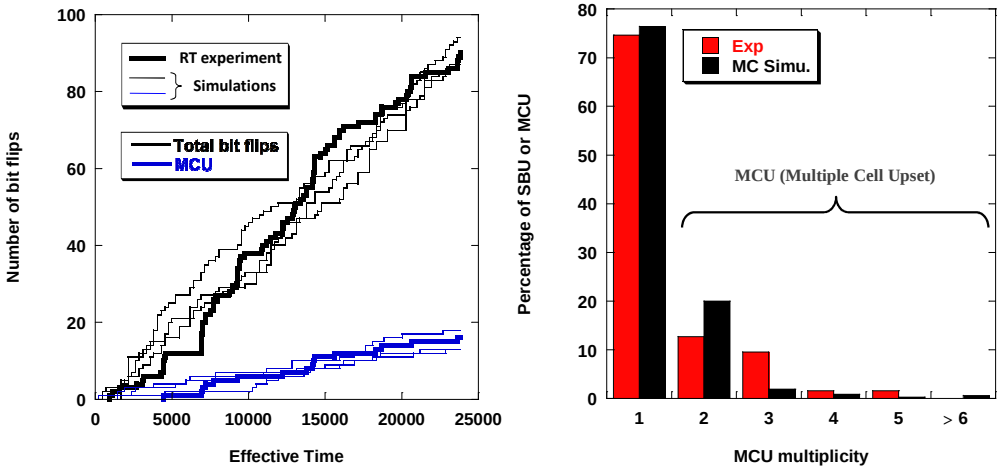


Figure 30. Left: Cumulative number of bit flips versus test duration for an underground real-time SER testing of 3.2 Gbits of 65 nm single-port SRAM (bold line). Several error distributions (thin lines) obtained by Monte Carlo simulations for 0.1 ppb of ^{238}U contamination in silicon are also shown. Rigth: Corresponding distributions of multiple cell upsets (MCU) as a function of event multiplicity deduced from both experiment and simulation. After Martinie et al. [135]. © 2012 Institute of Electrical and Electronics Engineers Inc.

In addition and as noted by Clark [136] the trend towards flip chip and 3D–IC architecture, in particular, has increased the need for reliable low alpha packaging materials. In these designs, packaging features such as wafer-level solder bumps and copper pillar solder caps are located close to the transistors of the device. This increases the transistor vulnerability to alpha emissions from these features and can lead to higher soft error rates. Figure 31 shows the acceptable alpha emission limits for packaging materials as a function of the technological node. These projections illustrate the transition from standard low alpha (LA) to ultra-low alpha (ULA) and even to super ultra-low alpha (SULA) that characterizes the recent evolution of the

microelectronics when entering in the nanometer area. Efforts to synthesize (chemical aspects) and characterize (metrology tools) such ULA/SULA materials certainly represents a challenge for all the microelectronic industry.

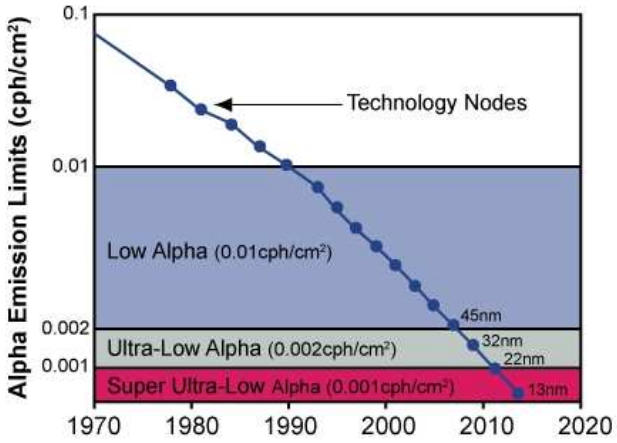


Figure 31: Acceptable alpha emission limits for packaging materials as a function of the technological node. Courtesy of Honeywell International Inc. [137].

4.4 Emerging devices and related mechanisms

4.4.1 Silicon-on-Insulator (SOI) technologies

SOS (Silicon-on-Sapphire) and SOI technologies have been initially proposed as a solution to the problem of bulk devices sensitivity to ionizing irradiations [138]. In bulk silicon devices, more than 99.9% of the substrate volume is not used and becomes a source of parasitic effects, such as leakage currents, latch-up, etc. The SOI materials eliminate this inconvenience, since the SOI structure itself is based on the principle of separation between the active region (the silicon film) and the inactive substrate by a more or less thick insulator layer (the buried oxide). Then, there is no parasitic PNPN structure leading to single-event latchup (SEL) in CMOS/SOI devices. In the 1970s and 1980s, SOS and SOI technologies were primarily (exclusively) used for space and military applications. But, besides their natural radiation hardness, it was observed that the parasitic capacities of SOI MOS devices are lower than those of bulk MOS devices, due to the existence of the buried oxide. This leads to enhanced speed performances for SOI circuits. Later, it was shown that the power dissipated in SOI technologies is strongly reduced compared to bulk Silicon, and that higher integration density is obtained with SOI. All these advantages make SOI technologies to gradually become a very attractive candidate for VLSI integrated circuits fabrication. After more than three decades of materials research and device studies, SOI wafers have definitively entered into the mainstream of semiconductor electronics. SOI MOSFET shows enhanced short-channel effects immunity and offers new potentiality for extending silicon devices into the nanometer region (sub-20 nm channel length). Concerning the sensitivity to radiation, the charge collection in SOI devices is limited to the silicon film which is very thin compared to bulk silicon devices. This makes SOI device naturally hardened to single-event effects. However, the unique configuration of SOI MOSFET's is responsible for novel mechanisms (such as floating-body) not occurring in the bulk silicon technology. The floating-body is at the origin of several parasitic phenomena specific to SOI devices like drain current overshoots and undershoots [139-140] or bipolar amplification. This last phenomenon is essential for the sensitivity of SOI devices and circuits to single-event [141-144]. As it will be explained in the following, SOI devices are not inherently immune to the radiation environment due to bipolar amplification, although they have less sensitive volume than bulk Silicon devices.

Bipolar amplification. There are two major types of SOI NMOS and PMOS transistor structures: fully depleted and partially depleted. The full or total depletion of the film depends on the silicon film thickness and doping level. Fully depleted (FD)

SOI devices are usually designed with very thin films that are totally depleted in standard operation mode. In partially depleted (PD) SOI MOSFETs with submicron length, the lateral bipolar transistor (source-body-drain) can be easily turned on. The basic mechanism of the bipolar amplification is the following: the heavy-ion strike on the device creates electron-hole pairs in the Silicon film. While minority carriers recombine quickly, the lifetime of majority carriers in the body region can be very long. Majority carriers that do not recombine can drift toward the source region and raise the body potential. Then, the source-to-body potential barrier is lowered, which triggers the lateral parasitic bipolar transistor inherent to the SOI transistor. The potential raise is maintained until majority carriers are recombined. The bipolar current amplifies the collected charge and decreases the SEU/SET immunity, especially at low LET [145]. This effect is further enhanced by impact ionization mechanism induced by the high electric field at the body-drain junction. The consequence is that the SOI immunity to radiation is degraded; although SOI devices have a smaller sensitive volume than bulk silicon devices, this is counterbalanced by the enhanced bipolar amplification [141-144].

To reduce these bipolar effects, the most common technique involves the use of body ties (which connect the floating body region to a fixed potential). The excess holes created by the ion strike no longer accumulate in the floating body region because they are evacuated through the body contact. This reduces considerably the parasitic bipolar transistor effects. However, body ties do not completely eliminate the bipolar effect; a voltage drop exists along the body tie due to its finite resistance, and the reduction of bipolar effect is less effective. The ability of body ties to suppress the bipolar effect strongly depends on the location of the body tie in relation to the ion strike [146]. The farther the ion strike is from the body tie, the larger the effect of the parasitic bipolar transistor [141], [144], [147-148].

Bipolar amplification can also occur in fully depleted transistor circuits. Previous experimental and theoretical studies have shown that, generally, fully depleted SOI-based devices exhibit reduced floating body effects and then lower bipolar amplification of the collected charge than partially-depleted SOI devices [141], [149-150]. The bipolar transistor mechanism in fully depleted devices has been explained in [151] using Monte Carlo simulations of 0.25 µm fully depleted SOI circuits: after irradiation of a n-channel MOSFET biased in its off state, excess holes are accumulated in the channel (mainly near the gate oxide) and lower the potential barrier; then electrons diffuse from source to drain to maintain the electrical neutrality. This mechanism is comparable to the bipolar transistor effect in partially depleted SOI devices [141-142]. Because bipolar amplification is less important for fully depleted than for partially depleted transistors, circuits based on fully depleted transistors are less sensitive to single-event upset than partially depleted circuits [150].

The effect of the parasitic bipolar transistor in SOI devices is quantified using a metric called the “bipolar gain”, β. The bipolar gain corresponds to the amplification of the deposited charge and is given by the ratio between the total collected charge, Q_{col}, at the drain electrode and the deposited charge, Q_{dep}:

$$\beta = \frac{Q_{coll}}{Q_{dep}}$$

Equation 11

The total collected charge at the drain electrode is obtained using the equation:

$$Q_{coll} = \int_0^t I_D dt$$

Equation 12

Where I_D is the drain current transient induced by the ionizing particle.

The deposited charge in a SOI device is calculated as a function of the particle LET using the following equation [152]:

$$Qdep[fC] = 10.3 \times LET[MeV/(mg/cm^2)] \times t_{Si}[\mu m]$$

Equation 13

where t_{Si} is the Silicon film thickness and 10.3 is a multiplication factor for Silicon (calculated using the Silicon density and the energy needed for creating an electron-hole pair in Silicon – 3.6 eV – [152]). In this equation a normal incident ion strike is considered and the LET is supposed constant along the ion path in the active Silicon film.

The transient response to radiation of FD SOI devices have been addressed in literature in numerous studies. For example, in [153], the drain current transient and the bipolar amplification of FD SOI MOSFETs with 50 nm and 80 nm gate length submitted to heavy-ion irradiation has been studied using both measurements and 3-D numerical simulations. The tested devices are floating body (without body contacts) NMOS transistors fabricated with a fully depleted (FD) single-gate SOI technology [154]. The transistors have been processed with a mid-gap TiN gate, and the Silicon film is nearly intrinsic (P-type, 10^{15} cm^{-3}). The thicknesses of the Silicon film and of the buried oxide are 11 nm and 100 nm respectively and the equivalent gate oxide thickness is close to 1.8 nm. 3-D numerical simulation results have been compared to experimental data measured by heavy ion experiments performed at GANIL (Grand Accélérateur National d'Ions Lourds, Caen, France). A detailed description of the experimental set-up and measured data can be found in [153]. Simulated drain current transients due to the ion strike have been normalized to their peak value and have been compared in Figure 32 to the initial Gaussian time-dependent charge generation. At low injection regime (LET=0.1 MeV/(mg/cm^2)), the drain current transient is almost synchronous with the charge generation, which illustrates a weak bipolar amplification. At high LET, the drain current peak is shifted and clearly wider than the Gaussian generation, indicating a significant bipolar amplification. The transient tail is longer for LET=4 MeV/(mg/cm^2) than for LET=100 MeV/(mg/cm^2), as a consequence of a more important floating body effect and bipolar amplification of the injected charge at medium LET. The transient tail increases from 0.1 MeV/(mg/cm^2) to 4 MeV/(mg/cm^2) and decreases then for higher LET.

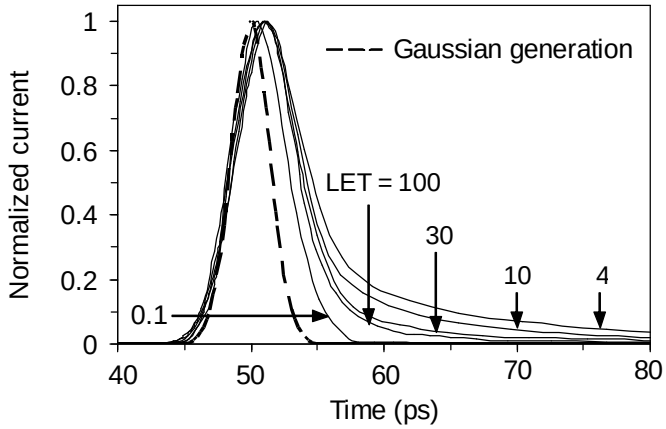


Figure 32: Drain current versus time in the quantum case at different LET values expressed in MeV/(mg/cm^2). The drain current transients are normalized to their peak value. The initial Gaussian charge generation is also reported for comparison. The ion track generation has a Gaussian shape versus time (characteristic time of 2 ps), centered at 50 ps and having an angle of incidence of 60°. After Munteanu et al. [153]. © 2006 Institute of Electrical and Electronics Engineers Inc.

The bipolar gain variation with the LET value (plotted in Fig. 33 together with experimental results for LET= 30 MeV/(mg/cm^2) reflects exactly the transient duration behavior as a function of LET. The maximum bipolar amplification is found for LET value around 4 MeV/(mg/cm^2). The bipolar gain decreases when the LET increases because the parasitic bipolar transistor enters in the high-injection regime, corresponding to high-current density. Then, the impact ionization generates more holes, which significantly increases the total hole concentration in the body and the parasitic bipolar gain decreases. The experimental bipolar gain was found to be 2.6 for 80nm gate length FD SOI transistors for a collected charge of 18 fC and a

maximum deposited charge of 6.8 fC. This gain value is consistent with the gain of 6.6 found with pulsed laser irradiation performed on L=50 nm gate length transistors fabricated with the same technology [149]. If one consider the 1/L behavior of the parasitic gain observed in SOI technologies [143], [155] a very good fit can be found between the two gain values.

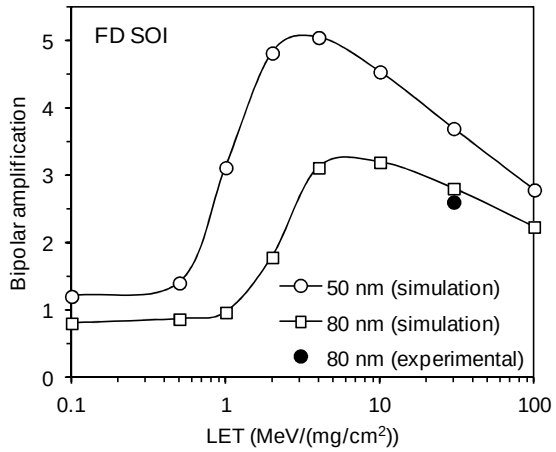


Figure 33: Bipolar gain in FD Single-Gate SOI devices for two gate lengths: 50 nm (70 nm drawn gate) and 80 nm (100 nm drawn gate). Both quantum and classical simulations are considered. The experimental bipolar gain obtained at LET=30 MeV/(mg/cm^2) on 80 nm FD SG SOI device is also reported. The angle of incidence in both experiment and simulation is 60°. The transistor is off-biased with V_D=0.7 V. After Munteanu et al. [153]. © 2006 Institute of Electrical and Electronics Engineers Inc.

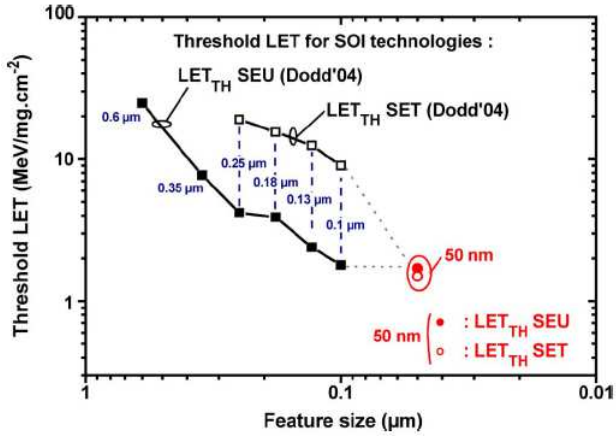


Figure 34: Simulated critical LET for unattenuated transient propagation (LET$_{TH\text{-}SET}$, open symbols) and SEU threshold LET (LET$_{TH\text{-}SEU}$, filled symbols) as a function of scaling for SOI CMOS technologies. Our results (50 nm, circles) are superimposed on mixed mode simulation from [38] (squares). After Gaillardin et al. [156]. © 2007 Institute of Electrical and Electronics Engineers Inc.

Scaling trends concerning the sensitivity to SEU in SOI static memory cell and the propagation of DSETs in SOI circuits have been addressed by Gaillardin et al. [156] using Mixed-mode simulations. In this approach, all devices (FD SOI NMOS and PMOS transistors with 50 nm-gate length and 3 µm gate width) have been modeled in full 3-D, then connected and only the OFF-NMOS is struck by an ionizing particle. The SEU threshold of memory cells (LET$_{TH\text{-}SEU}$) and the DSET critical LET for unattenuated propagation in chain of inverters (LET$_{TH\text{-}SET}$) have been analyzed. The SEU threshold LET was determined by varying the ion strike LET until the static memory cell was observed to upset. The authors have added the LET$_{TH\text{-}SEU}$ obtained for 50 nm FD SOI technology to data presented by Dodd et al. [38] on former SOI technologies, as shown in Figure 34. The results obtained in [156] showed that threshold LET of 50 nm devices stands at a similar value than that of the previous technology node (LET$_{TH\text{-}SEU}$=2 MeV/(mg/cm^2)). As explained in [156], the reduced

sensitive volume associated to the efficient electrostatic potential control provided by the gate in the body mitigate the effects induced by a ionizing particle hit in this advanced 50 nm FDSOI technology. The LET_{TH-SET} for unattenuated transient propagation in a chain of inverters was also studied in [156] as a function of device scaling (Fig. 34). The results obtained for the FD SOI 50 nm chain of inverters were in good agreement with data from the literature [38]. In was shown that contrary to the SEU threshold LET, LET_{TH-SET} decreases with technology scaling [156]. The speed of these circuits increases with size reduction and is sufficient to propagate shorter transients [43], [157] (less than 100 ps wide in sub-0.1 µm technologies) that become indistinguishable from normal circuit signals [156]. It is important to note that results concerning the 50 nm FDSOI devices in Fig. 34 have been obtained by simulation and need to be confirmed experimentally.

4.4.2 Multi-gate devices

Multiple-Gate nanowire MOS transistors (Fig. 1) are now widely recognized as one of the most promising solutions for meeting the roadmap requirements in the deca-nanometer scale [158]. A wide variety of architectures, including planar Double-Gate (DG) [159-160], Vertical Double-Gate, Triple-Gate (Tri-gate) [158], [161], FinFET [162-163], Omega-Gate (Ω-Gate) [164], Pi-Gate (π-Gate) [165], Δ-channel SOI MOSFET [166], DELTA transistor [167], Gate-All-Around (GAA) [158], [168], Rectangular or Cylindrical nanowires [169], has been proposed in the literature. These structures exhibit a superior control of short channel effects resulting from an enhanced electrostatic coupling between the conduction channel and the surrounding gate electrode. It has been shown that the electrostatic control is enhanced when increasing the "Equivalent Number of Gates" (EGN) from 2 (for Double-Gate devices, Fig. 35) to 4 (for Gate-All-Around devices where the gate electrode is wrapped around the entire channel, Fig. 35). In this way, Multi-Gate devices could be designed with intrinsic channels, offering then an enhanced mobility, the elimination of doping fluctuations and a high probability of ballistic transport. Further, for the symmetrical DG device, the condition of “volume inversion” [170] can be beneficial with regard to carrier mobility and source-drain transport.

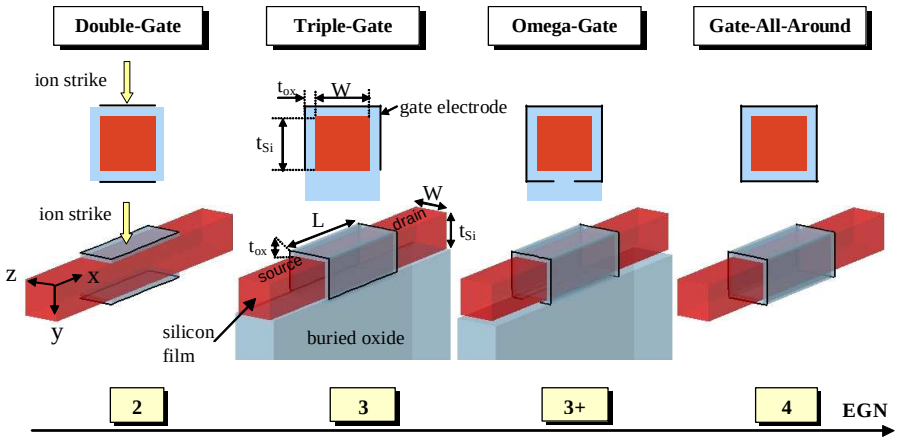


Figure 35: Schematic description of the Double-Gate, Triple-Gate, Omega-Gate and GAA structures and their main geometrical parameters. The devices are classified as a function of the "Equivalent Gate Number" (EGN). The schematic cross-sections in the (y-z) plane are also shown. After Munteanu et al. [171]. © 2007 Institute of Electrical and Electronics Engineers Inc.

In order to further enhance the on-state current over the off-state current ratio (I_{ON}/I_{OFF}) and to achieve a higher current drivability compared to conventional single channel devices, 3-D vertically stacked nanowire MOSFETs with multiple-gate operation, also called Multi-Channel Nanowire MOSFETs (MC-NWFET) have been recently proposed [172-173]. MC-NWFETs (Fig. 35) combine the advantages of excellent control of short-channel effects with a high on-state current due to a multiple-gate architecture and the 3-D integration of vertically stacked channels. GAA devices with ultra-thin and narrow channels (about 10 nm) are seen as the ideal architecture for off-state current control of sub-10 nm gate lengths [172]. Meanwhile, the current density per surface of such a device is limited by the lithography pitch,

which dictates the distance between nanowires. The current density can be improved by the vertical integration of GAA devices. Thanks to the integration of vertically stacked channels, a 5× increase in current density per layout surface can be achieved compared to planar transistors with the same gate stack [172].

The transient response of Multi-Gate devices submitted to heavy ion irradiation has been investigated in literature by both experimental and 3-D numerical simulation. These previous studies demonstrate that Multi-Gate devices show better radiation hardness than fully-depleted Single-Gate SOI transistors, particularly due to the enhanced control of the body potential and of the reduction of floating body effects. Simulation studies also show that the transient and charge collection are very fast in Multi-Gate devices due to the small active volumes that allow all the excess charge to be quickly evacuated. However, these very fast transients are specific to intrinsic devices and can be degraded by extrinsic elements related to fabrication process which may not be mature in Multi-Gate technologies. An example is shown in [156], where the radiation-induced current transient of Omega-Gate devices has been found sensibly longer than that of single-gate FD SOI devices due to the technological process which includes long resistive access to source and drain electrodes. If the length of this region increase, the carriers produced in the body need more than time to reach the drain electrode [156]. Consequently, the current transient is broader, with a large width of ~ 64 picoseconds at half maximum (FWHM) values, and the transient tail is longer. Consequently, these devices collect a higher total charge than planar FD SOI devices with similar gate lengths [156]. This long transient is not an intrinsic characteristic of Omega-Gate devices. Thus, the length of the highly doped access area which connects the channel to the drain (source) electrode is a key issue for the radiation-induced current transient and then access regions have to be carefully optimized in order to conserve the intrinsic radiation-hardness of Omega-Gate devices [156].

The number of equivalent gates is also a key-parameter for radiation-induced response of Multi-Gate devices. Figure 36 shows a collection of drain current transients in different Multi-Gate devices obtained by 3-D numerical simulation. These results indicate that the peak value of the drain current transient is reduced when EGN increases. When EGN increases, the channel is better controlled by the gate and the floating body effects are strongly reduced. The drain current transient tail is logically shorter when going from DG to GAA devices. Simulation results in [171] also shown that the bipolar amplification decreases when increasing EGN due to less floating body effects. However, the difference between the different architectures of Multi-Gate devices is strongly reduced at high LET as the charge generated by the ion strike is high enough to collapse the electric field at the body-to-drain junction and to reduce the bipolar amplification.

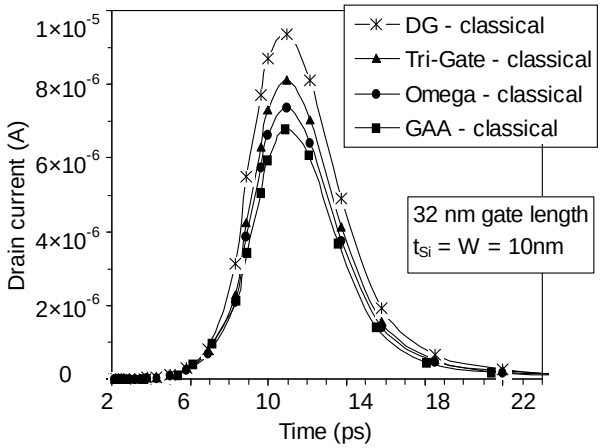


Figure 36: Drain current transients induced by an ion strike vertically (y direction) in the middle of the silicon film in DG, Tri-Gate, Omega-Gate and GAA devices. The ion track generation has a Gaussian shape versus time (characteristic time of 2 ps), centered at 10 ps and a LET = 1 MeV/(mg/cm^2). The simulated devices are 32 nm gate length MOSFETs. After Munteanu et al. [171]. © 2007 Institute of Electrical and Electronics Engineers Inc.

The scaling of Multiple-Gate MOSFET requires the use of an increasingly thinner Silicon film, for which new phenomena have to be taken into account, such as quantum-mechanical confinement. These phenomena induce a strong subband splitting and the carrier confinement in the narrow potential well formed by the Silicon film [174]. Quantum effects sensibly modify the three dimensional (3-D) carrier distribution in the channel, the most important effect being the shift of the charge centroid away from the interfaces into the Silicon film. The inversion charge and then the drain current are reduced in the quantum case with respect to the "classical" case (i.e. without quantum effects). Quantum-mechanical confinement is stronger when the film is thinner. It has been shown that the energy quantization becomes important for channels below 10 nm thick, for which it becomes mandatory to take into account quantum effects in the device simulation. In Single-Gate or Double-Gate configurations, carriers are confined in a single direction (vertically, perpendicular to the gate electrode and to the source-to-drain axis). In multiple-gate architectures, and especially in Gate-All-Around devices, the quantum-mechanical confinement is stronger because the carrier energy is quantified in two directions (vertically but also horizontally, in both directions perpendicular to the gates electrodes and to the source-to-drain axis). Then, the carrier confinement and its effects (such as the reduction of the total inversion charge) are stronger in Multiple-Gate devices with EGN≥3 than for single-gate or double-gate architectures.

The impact of quantum confinement on the radiation response of Multi-Gate devices has been studied by quantum numerical simulation in [171]. In that study, the gate length has been reduced from 32 to 20 nm and the corresponding film thickness has been thinned from 10 nm to 5 nm (Table 2). The bipolar amplification of these Multi-Gate devices, reported in Table 2, is very low compared with fully depleted SOI-based devices because in Multiple-Gate devices the control of the channel by the gates is naturally reinforced, and strongly reduces the floating body effects. As stated above, the bipolar amplification decreases when increasing the number of gates from the Double-Gate to the GAA structures. However, the difference between the four architectures is reduced for the 20 nm-gate length devices compared with the 25 nm and 32 nm ones, due to the very thin square wire cross-section (t_{Si}=W=5 nm). When decreasing the cross-section, the influence of the gate configuration is attenuated and the values of the bipolar gain for the different structures are almost the same. This behavior can be explained by the fact that, around 5 nm and below, the combination of gate electrostatic control and quantum mechanical confinement leads to similar carrier density distributions in the film for all gate configurations [16]. At this ultimate scale of integration, it should be expected that the sensitivity of all multiple-gate nanowire architectures (EGN≥2) to heavy ion irradiation sensibly become equivalent.

Gate length	W=t_{Si}	Structure	EGN	Bipolar gain
32 nm	10 nm	Double-Gate	2	1.79
		Tri-Gate	3	1.49
		Omega-Gate	3+	1.3
		GAA	4	1.18
25 nm	8 nm	Double-Gate	2	1.53
		Tri-Gate	3	1.21
		Omega-Gate	3+	0.94
		GAA	4	0.82
20 nm	5 nm	Double-Gate	2	0.82
		Tri-Gate	3	0.78
		Omega-Gate	3+	0.73
		GAA	4	0.72

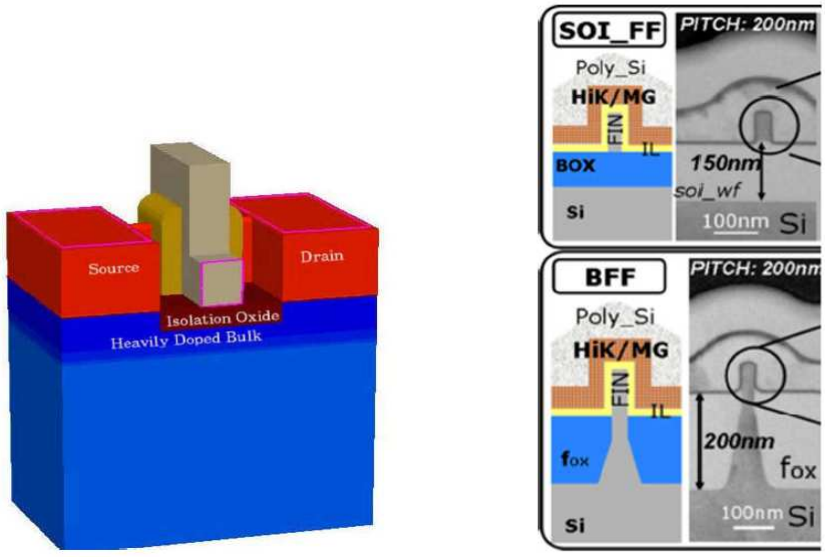
Table 2: Bipolar gain in multiple-gate nanowire MOSFETs as obtained by quantum 3-D numerical simulation. After Munteanu et al. [171].

Concerning the radiation-hardness of circuits based on Multi-Gate devices, only very few studies are available in literature. Recently, Seifert et al. [175] reported on radiation-induced SER measured on SRAM logic circuits based on 22 nm Tri-Gate devices technology. This work shows that the SER of SRAM and sequential elements is reduced in the order of 1.5× to 4× in 22 nm Tri-Gate compared against 32 nm planar devices for high energy neutrons and protons [175]. The SER reduction is even larger for alpha-particle (10× lower), which shows that alpha-particle SER has become negligible in the investigated technology [175]. This study confirms the benefits of Multi-Gate devices in terms of radiation-hardness compared to planar bulk technology [175].

4.4.3 Bulk and SOI FinFET

Generally, FinFETs are manufactured on SOI substrates [176-177]. However, many disadvantages characterize SOI wafers compared to bulk wafers, such as the problems of self-heating, cost, density of defect, etc. Bulk substrates, besides eliminating most disadvantages of SOI, are compatible with existing planar CMOS technological process and reduces considerably the manufacturing costs. This explains the great interest to fabricate FinFETs on bulk wafers [178]. Figure 37 (a) shows the 3-D structure of a typical bulk FinFET; the comparison between bulk and SOI FinFET architectures is illustrated in Fig. 37 (b).

Concerning radiation effects, the performances of bulk FinFET compared to SOI FinFET are really mitigated, as illustrated in recent publications. The transient responses of bulk and SOI FinFETs have been studied by El-Mamouni et al. [179] using top-side Single Photon Absorption (SPA). In this work, it was reported that the charge collection of PMOS SOI FinFETs is lower than that of similar bulk devices. Transients measured on bulk FinFET devices were found larger and longer than those of the SOI FinFETs. SOI FinFETs also have a smaller volume of collection than their counterparts on bulk due to the buried oxide layer which isolates the active layer from the substrate. Consequently, the collection volume of a SOI FinFET transistor is limited to the fin, while the collection volume of a bulk FinFET extends in the well region too.



(a) (b)

Figure 37: (a) 3-D view of simulated bulk FinFET showing the patterned 3-D gate and bulk doping layer. After Manoj et al. [178]. © 2008 Institute of Electrical and Electronics Engineers Inc. (b) SEM picture (right) and cross section (left) of a FinFET device. The SOI FinFET is on the top and the bulk FinFET is on the bottom. After Chiarella et al. [180].

Additional measurements using laser testing have been reported in [181], where it is shown that charge collection in 130 nm bulk p-channel FinFETs strongly depends on the structure of the drain region. In this paper is reported that, in the devices tested, charge collection in the drain region masks the contributions of the fins to the charge collection process [181]. The drain/substrate p-n junction efficiently collects charge

generated in the substrate [181]. Carriers generated in the substrate below the drain junction also can diffuse to the drain junction where they are collected. Heavy-ion-induced charge collection measurements in n-channel bulk FinFETs showed that the greatest amount of collected charge occurs for strikes in the drain region [181]. Device scaling affects the geometry of the fin, but the drain (and source) region may dominate charge collection [181].

Finally, heavy ion-induced charge collections obtained from sub-70 nm bulk and SOI FinFETs with both conventional and reduced-area drain regions (saddle layout) have been recently reported by El-Mamouni et al. in [182] (Fig. 38 (a)). Drain current transient measured on these devices are reported on Fig. 38 (b).

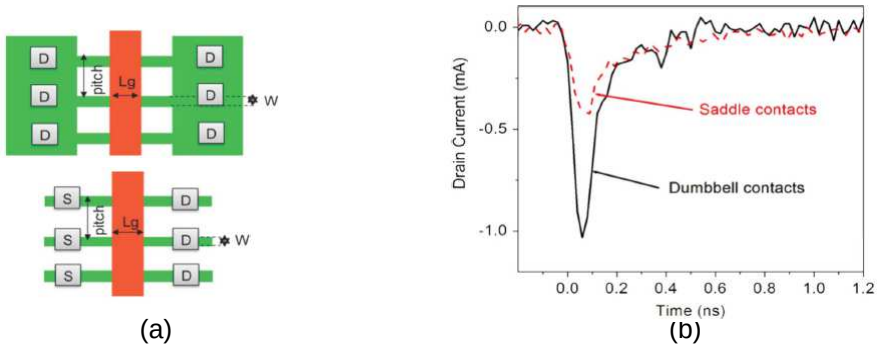


Figure 38: (a) Top layout view of FinFETs with : (top) common drain contact (dumbbell contact) and (down) multiple drain contacts (saddle contact). FinFETs with dumbbell and saddle contacts are designed with different numbers of fins in the structures used in this study.. After El-Mamouni et al. [182]. (b) Measured drain current transients with dumbbell contact and saddle contact. After El-Mamouni et al. [182]. © 2012 Institute of Electrical and Electronics Engineers Inc.

The amount of charge collected in bulk FinFETs with saddle contacts is at least 17% less than that collected in bulk FinFETs with dumbbell contacts [182]. This result is extremely important when values of critical charge are on the order of 1–10 fC, as shown in [183]. The shunt effect plays a key role in the charge collection process in the investigated bulk and SOI FinFETs [182]. The small feature size allows the ion track to affect the whole channel region. SOI FinFETs exhibit higher tolerance to SEEs in comparison to their bulk counterparts. The results presented here suggest that improved designs of the drain region will significantly increase bulk FinFET SEE tolerance [182]. Charge collection in SOI FinFETs with dumbbell and saddle contacts show a strong dependence on the substrate bias, with the highest amount of charge collected when the substrate is negatively biased [182]. This effect can decrease the SEE tolerance of SOI devices [182].

4.4.4 Multi-gate and Multi-Channel devices with independent gates

In spite of excellent electrical performances due to their multiple conduction surfaces, conventional Multiple-gate MOSFETs or Multi-Channel (MC) Nanowire (NW) MOSFETs (MC-NWFETs) provide only three-terminal (3T) operation because devices are designed with a single gate electrode (surrounding the channel) or, in the case of Double-Gate devices, the two gates are tied together. Planar Double-Gate, FinFET and MC-NWFET structures with independent gates have been recently proposed [184-190], that makes possible a four terminals (4T) operation. These devices offer novel potentialities, such as a dynamic threshold voltage control by one of the two gates, transconductance modulation, signal mixer, in addition to the conventional switching operation. Thus, 4T-DGFET, 4T-FinFET and 4T-MC-NWFET are promising for future high performance and low power consumption integrated circuits. The schematic structures of these different architectures are illustrated in Figure 39.

The radiation response of independent-gate devices have been studied by 3-D numerical simulation in [191] and [192] and compared to their 3T devices counterparts. Figure 40 (top) shows the influence of the second gate bias on the electron density profile (static simulation) in DGFET: in 3T-DGFET the electron density is symmetrical with respect to the two gate interfaces, but the symmetry is broken in 4T-DGFET by the second gate bias. The static drain current is also deeply

modified by the bias of the second gate, as shown in Fig. 40 (bottom) for FinFET devices. The off-state current of the 4T-FinFET is lower than that of the 3T-FinFET for negative V_{G2} and higher for positive V_{G2}.

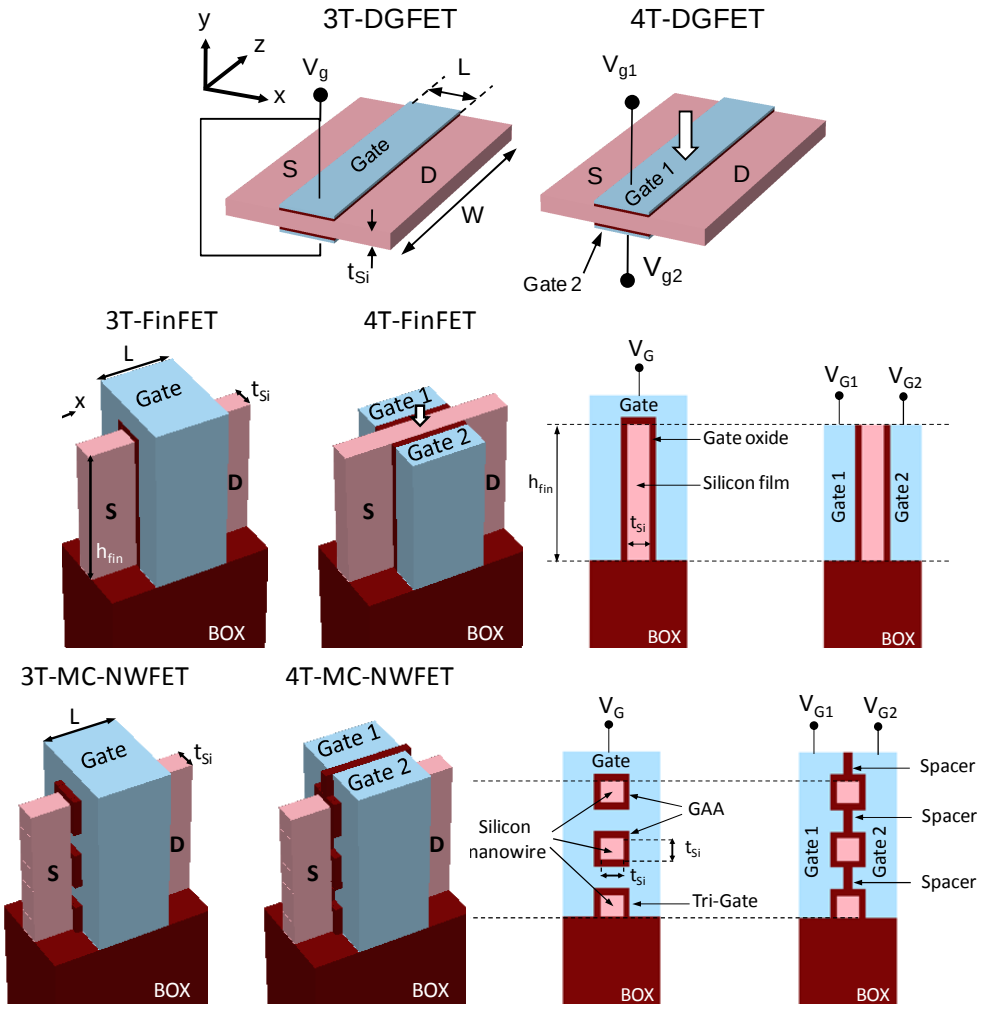


Figure 39: Schematic description of the 3-D Double-Gate, FinFET and MC-NWFET structures with three and four terminals. The main geometrical parameters used in simulation are also defined (S=source region and D=drain region). Schematic cross-sections in the (y-z plane) showing the bias conditions specific to each device are also shown. For MC-NWFET structures, this figure also indicates the particular devices which compose the nanowire stack. After Munteanu et al. [191-192]. © 2009 & 2012 Institute of Electrical and Electronics Engineers Inc.

Concerning the radiation-induced drain current transients, simulation results show that the peak of the drain current transient in 4T-FinFET is higher than in 3T-FinFET for positive V_{G2} and smaller for negative V_{G2}. The results obtained in [191] and [192] also show that the collected charge and the bipolar amplification (see Figure 41) are higher in 4T than in 3T devices for both positive and negative back gate bias, for low and intermediate LET (lower than about 5 MeV/(mg/cm^2)). This is due to a better control of the electrostatic potential in the channel by the front gate in 3T devices, which reduces the floating body effects. These results are shown in Fig. 41 (a) for FinFET devices and in Fig. 41 (b) for MC-NWFET. For LET values higher than 5 MeV/(mg/cm^2), the bipolar gain becomes the same for all devices. In 4T devices the bipolar gain increases with the increase of positive V_{G2} and with the decrease of the negative V_{G2}. Finally, the bipolar gain is found higher for negative V_{G2} than for positive V_{G2} due to a lower SRH recombination rate.

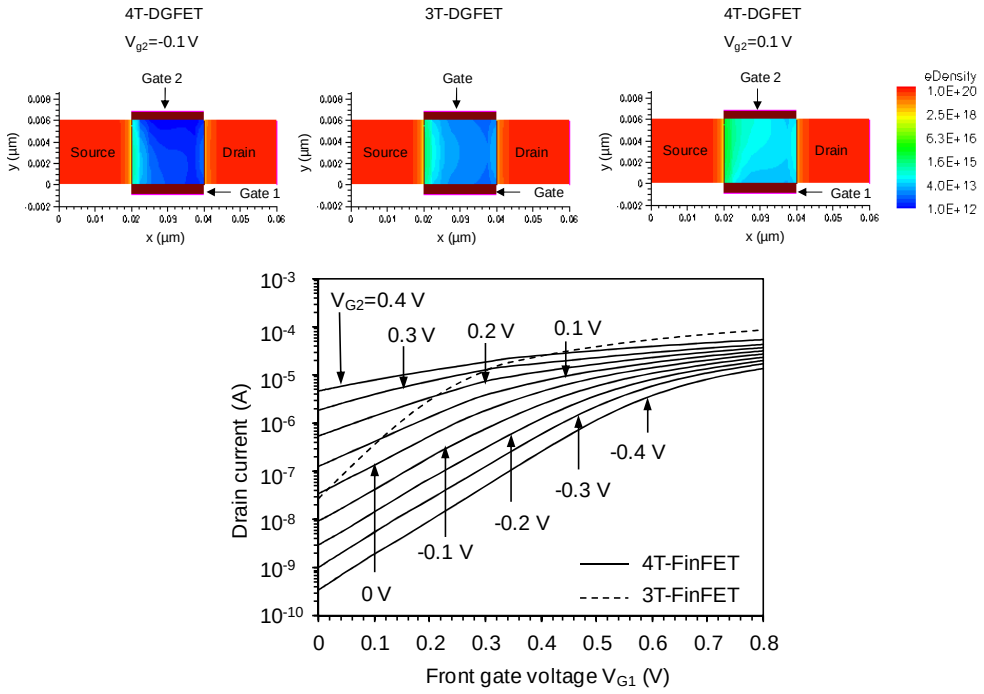


Figure 40. Top: 2-D profile of electron densities in a vertical cross-section (plane x-y) in the middle of the channel in 3T-DGFET and 4T-DGFET biased at V_{G2}=-0.1 V and V_{G2}=0.1 V. V_D=0.7 V. After Munteanu et al. [191]. © 2009 Institute of Electrical and Electronics Engineers Inc.Bottom: Drain current characteristics as function of V_{G1} for 4T-FinFET with different back gate biases V_{G2}. The drain current versus V_G of 3T-FinFET is also reported for comparison. For all curves V_D=0.8 V and V_S=0 V. After Munteanu et al. [192]. © 2012 Institute of Electrical and Electronics Engineers Inc.

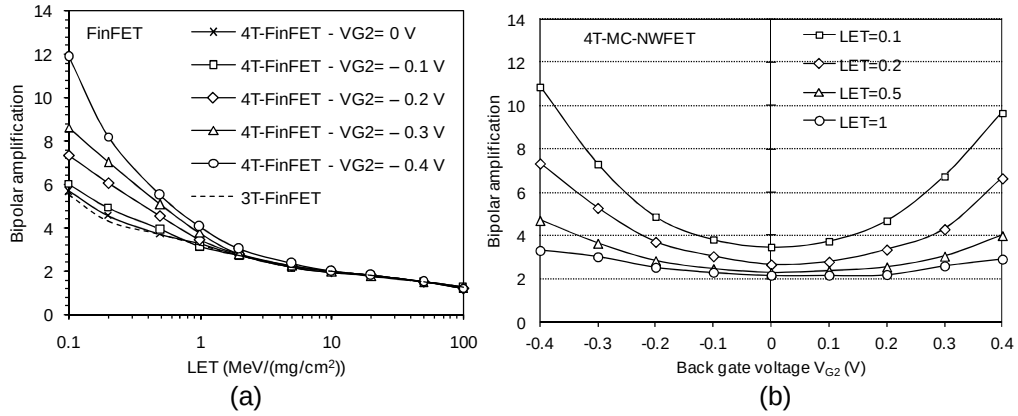


Figure 41: (a) Bipolar amplification as function of LET in 3T-FinFET and 4T-FinFET at different back gate biases. (b) Bipolar amplification at low LET values as function of V_{G2} in and 4T-MC-NWFET. The LET values are expressed in MeV/(mg/cm^2). After Munteanu et al. [192]. © 2012 Institute of Electrical and Electronics Engineers Inc.

4.4.5 III-V FinFET and Tunnel FET

In order to improve CMOS performances, especially on-state current, as ITRS recommendation for future technological nodes, high mobility materials have been recently investigated to potentially replace silicon in MOSFET's channel [193]. Due to low conductivity effective masses in both valence and conduction bands (which leads to higher holes and electrons mobilities than in Si), Ge and III-V materials like GaAs, InAs, InSb or ternary compounds are seriously considered in recent works to respectively enhance p-MOSFETs and n-MOSFETs performance for high-performance CMOS logic applications. The SEE sensitivity of III-V materials technologies has been firstly investigated in literature by McMorrow et al. in [194-196]. As explained by Dodd et al. [197], III-V materials technologies are often even more sensitive to SEU than their silicon counterparts due to internal gain mechanisms

which often result in high charge collection efficiency and hence enhanced SEE sensitivity. In addition, similar to advanced CMOS technologies, higher speed operation results in an increased sensitivity to SETs [197].

Steep switching devices such as Tunnel FET [198-200] have been proposed these last years for low voltage application. Tunneling FETs (TFETs) allows overcoming the fundamental subthreshold swing (SS) value of 60 mV/decade, an inherent limitation to conventional MOSFETs. This limitation is due to the use of a particular mechanism for carrier injection based in the band-to-band tunneling (BTBT) that appears in a gated p-i-n diode operating under reverse bias as the building block of existing TFET designs [201-202]. This allows a reduction in the supply voltage (needed for low voltage applications) and strongly reduces OFF-state currents in TFET, which makes these devices one of the most promising novel devices currently under study [201], [203-204]. Combining high-mobility materials with TFET could be seriously considered to reach predicted performances for low-power applications.

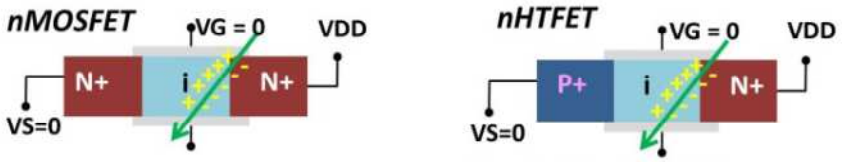


Figure 42: Schematic description of the simulated nMOSFET and nHTFET. Adapted from Liu et al. [205]. © 2012 Institute of Electrical and Electronics Engineers Inc.

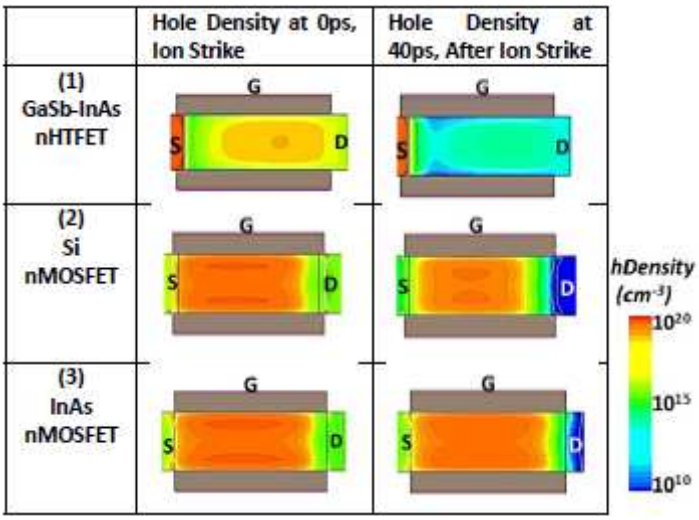


Figure 43: Time evolution of hole density in n-type device channel region. After Liu et al. [205]. © 2012 Institute of Electrical and Electronics Engineers Inc.

Transient error generation and transient drain current in III-V FinFET and III-V Hetero-junction Tunnel FET (HTFET) have been investigated by Liu et al. [205] using device and circuit simulation. The simulated MOSFET and HTFET structures are schematically represented in Figure 42. Figure 43 shows the time evolution of hole density before and after ion strike in n-type device channel region for the three simulated devices: Si nMOSFET, InAs nMOSFET and InAs nHTFET. In nMOSFET, the radiation-induced holes are stored in the body (due to the source barrier), which induces barrier lowering (Fig. 44 (left)) and increases the channel potential [205]. The, additional electrons flow into channel due to the parasitic bipolar amplification mechanism which further increase the drain node charge collection [205]. On the contrary, in HTFET, due to the asymmetric source and drain doping, both electrons and holes can be collected through the ambipolar transport [205]. This can be seen in Fig. 43 where the hole density in HTFET decreases fast due to ambipolar transport and the channel barrier is unchanged (Fig. 44 (right)) [205]. Holes and electrons can be collected at the source and drain respectively, which greatly reduces the body charge storage induced bipolar gain and further reduces the collected charge, the transient current (I_{Trans}) magnitude and transient duration (Fig. 44) [205].

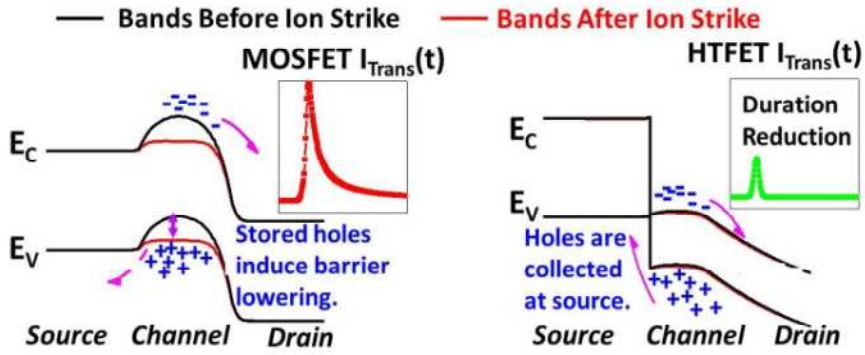


Figure 44: Band diagram of nMOSFET (left) and nHTFET (right) before and after ion strike. After Liu et al. [205]. © 2012 Institute of Electrical and Electronics Engineers Inc.

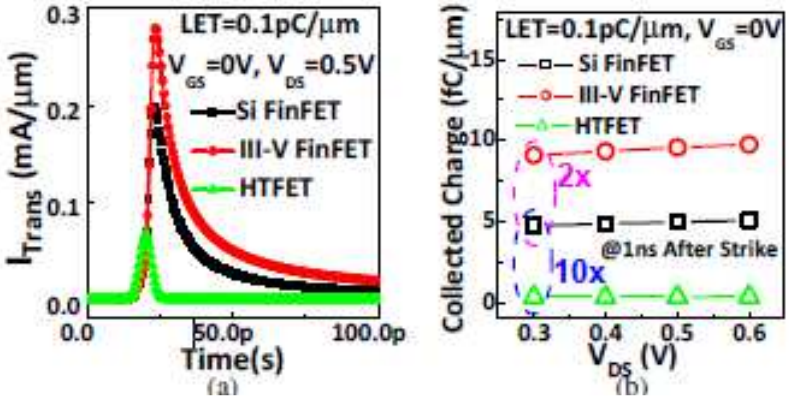


Figure 45: Radiation induced (a) transient current profile and (b) collected charge at 1ns (LET=0.1pC/µm) for each emerging device. After Liu et al. [205]. © 2012 Institute of Electrical and Electronics Engineers Inc.

Drain current transient are compared in Fig. 45 (a) [205] and the collected charge is plotted in Fig. 45 (b). These figures show that at LET=0.1pC/µm, the transient duration in HTFET is reduced by 80% and the collected charge is reduction by 90% compared to Si FinFET [205]. Figure 45 (b) also indicates that a 2× charge collection enhancement is obtained in III-V FinFET compared to Si FinFET due to high carrier mobility. The results obtained in [205] also indicate significant reduction in bipolar gain in HTFET compared to MOSFET. Then, HTFET shows reduced current magnitude and 10× charge collection reduction compared to Si FinFET [205].

SRAM SER and logic SER projections have been also investigated in [205] using a simplified analytical model. Results are summarized in Figure 46. As explained in [205], III-V FinFET shows increased charge deposition due to low ionization energy, which increases the SER for SRAM cell for all V_{DD} compared to Si FinFET [205]. For logic circuits, III-V FinFET shows reduced SER compared to Si FinFET below 0.5V due to improved latching window masking [205]. Concerning HTFET, these devices show superior radiation resilience compared to both Si and III-V FinFET over the voltage range of 0.3V-0.6V for both SRAM and logic [205]. As concluded in [205], this fundamental advantage stems from bipolar gain reduction, on-state enhanced Miller capacitance effect, and improved latching window masking, which makes HTFET desirable for radiation-resilient ultra-low power application.

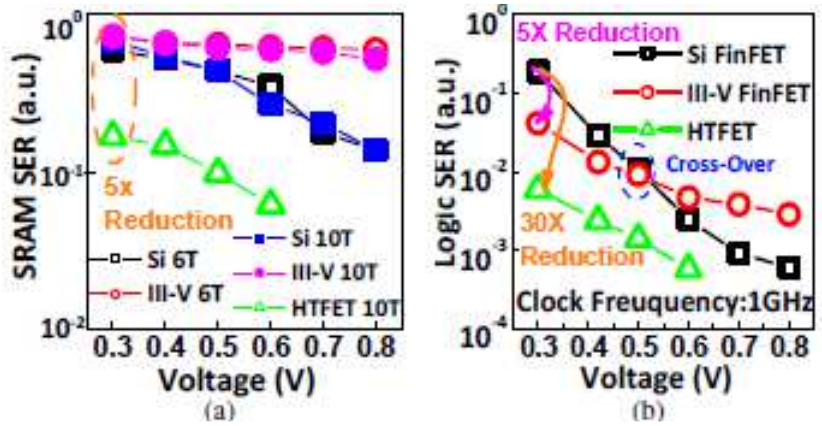


Figure 46: Relative SER for (a) SRAM and (b) Logic with voltage scaling. HTFET has superior soft error resilience for both SRAM and logic. IIIV FinFET logic shows lower SER below 0.5V over Si FinFET. After Liu et al. [205]. © 2012 Institute of Electrical and Electronics Engineers Inc.

4.4.6 Junctionless devices

Junctionless MOSFET, with a same type of semiconductor throughout the entire silicon film including the source, channel and drain regions, Fig. 47(b)], have been recently proposed [206-211]. A junctionless Double-Gate MOSFET (JL-DGFET) has a heavily doped silicon film sandwiched between two gates tied together. The two gates are used to control the electrostatic potential in the channel and then to switch on and off the device. Generally, the junctionless MOSFET fabrication is considerably simplified compared to conventional process since there are no doping concentration gradients in the device [209] and no semiconductor type inversion. The off-state current is then uniquely determined by the electrostatic control of the gates and not by the leakage current of the reversed-biased source-channel or drain-channel diode [206]. This could be very interesting for ultra-short devices typically for deca-nanometer channel lengths.

The operation of JL-DGFET is different from that of conventional inversion-mode (IM) DGFET. The classical field-effect MOS transistor is normally in the off-state if a conduction channel is not created under the gate. The junctions are reversely biased and the current flow is blocked. A voltage has to be applied on the gate in order to turn on the transistor. The vertical electric field created across the gate oxide attracts carriers to the interface creating an inversion channel and the carriers flow from the source to the drain through this channel. Then, in IM-DGFET, the electric field is highest when the device is turned on. On the contrary, the junctionless transistor is normally in the on-state and the current flows from the source to drain in the channel that extends over the entire silicon film [211]. In this transistor the work function difference between the gate and the doped silicon film leads to a positive flat band voltage. Then, in on-state the junctionless transistor is in flat band conditions and the transverse electric field is zero [211]. The electric field will be used to deplete the silicon film and turn off the transistor. Unlike IM-DGFET, the electric field is high in the off-state for JL-DGFET and very low in the on-state [209]. The conduction takes place in the film volume contrary to inversion-mode devices where the conduction takes place at the silicon/oxide interface. This could enhance the mobility in the on-state because the surface-roughness scattering is reduced. However, the high doping level in the channel of JL-DGFET is expected to induce larger floating body effects than in IM-DGFET where the channel is intrinsic. This could reduce the device immunity to single-event in spite of a good control of the channel potential by the two gates.

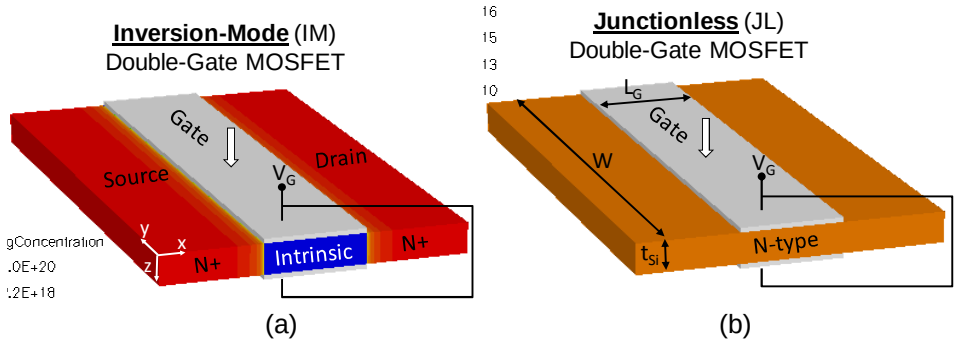


Figure 47: Schematic description of the simulated IM-DGFET (a) and JL-DGFET (b) structures. The main geometrical parameters are also defined. For a better view both the spacers and isolation oxide are not shown. After Munteanu et al. [212]. © 2012 Institute of Electrical and Electronics Engineers Inc.

From a radiation-hardness point of view, the high doping level in the silicon film of JL-DGFET could have a negative impact on its immunity to single-events, because the floating-body effects are expected to be strong. Then, in spite of its double-gate configuration, JL-DGFET should be more sensitive to radiation than IM-DGFET where the channel is intrinsic. The radiation-induced transient response of JL-DGFET was studied in [212] and compared to that of IM-DGFET with similar geometrical parameters. Figure 48 shows the drain current and collected charge transient resulting from the ion strike in IM-DGFET and JL-DGFET. The drain current decay after the ion strike is slower for JL-DGFET than for IM-DGFET. The reason is that the floating body effects are more important in JL-DGFET than in IM-DGFET. This is due to the high doping in JL-DGFET since the film is intrinsic in IM-DGFET. Then, the collected charge is higher in JL-DGFET than in IM-DGFET and increases for higher doping levels.

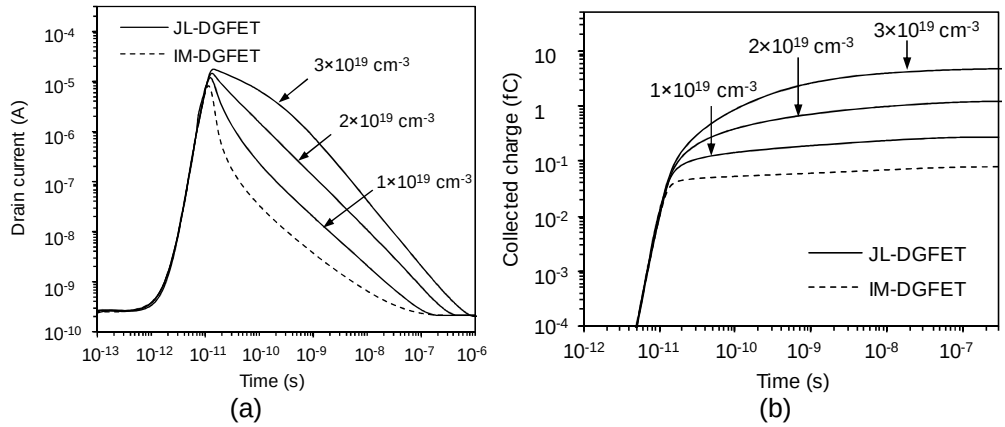


Figure 48: Drain current transient (a) and collected charge (b) in both IM-DGFET and JL-DGFET structures. The incident ion LET is 1 MeV/(mg/cm^2). V_G=0 V and V_D=0.75 V. The deposited charge is 5.98x10^{-2} fC. After Munteanu et al. [212]. © 2012 Institute of Electrical and Electronics Engineers Inc.

The bipolar amplification as function of LET is plotted in Figure 49. As expected, the bipolar gain was found higher for JL-DGFET than for IM-DGFET. The bipolar gain decreases when the LET increases because the parasitic bipolar transistor enters in the high-injection regime. At very high LET values, the bipolar gain in JL-DGFET decreases rapidly and reaches the value of the bipolar gain in IM-DGFET. When the channel doping increase, the floating body effects are enhanced and both the collected charge and bipolar amplification increase. Impact ionization has been also larger for higher doping levels, which additionally contribute to enhance the bipolar amplification. From these results, we could expect a worse immunity to single-event phenomena of JL-DGFET compared to IM-DGFET. This will probably have a consequence on the behavior under irradiation of circuits based on these devices. But single device behavior is not enough to determine the circuit sensitivity to single-events because this also depends on the load capacitance. More detailed study

concerning this point is needed to exactly quantify the sensitivity to single-event of JL-DGFET-based circuits.

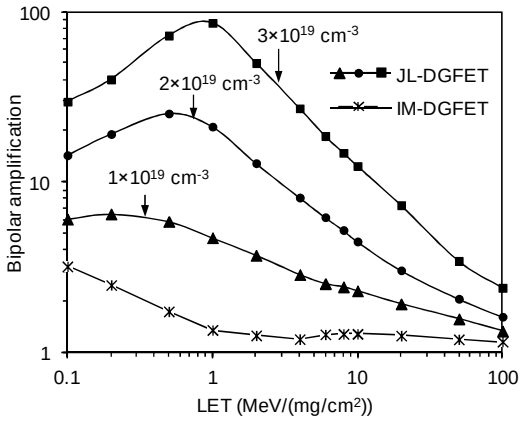


Figure 49: Bipolar amplification as function of LET in IM-DGFET and JL-DGFET. V_G=0 V and V_D=0.75 V. After Munteanu et al. [212]. © 2012 Institute of Electrical and Electronics Engineers Inc.

4.5 A "More than Moore" near-term perspective: 3D integration

To conclude this review in this last paragraph, we illustrate one of the more promising near-term perspective offered by the "More than Moore" issue: the 3D integration. Indeed, new developments in electronic system integration look increasingly to the third dimension for a variety of reasons, such as miniaturization, heterogeneous integration, improved circuit performance and lower power consumption [5]. A broad variety of technologies have been proposed to integrate circuits in 3D, including 3D monolithic (on Si) and 3D heterogeneous IC approaches. Figure 50 shows this historical trend in microelectronic device integration, from the first discrete components to 3D integrated circuits. The 3D stacked geometry as well as the heterogeneous nature of the future circuits raises a certain number of unresolved issues concerning their susceptibility to soft errors and more generally to single event effects.

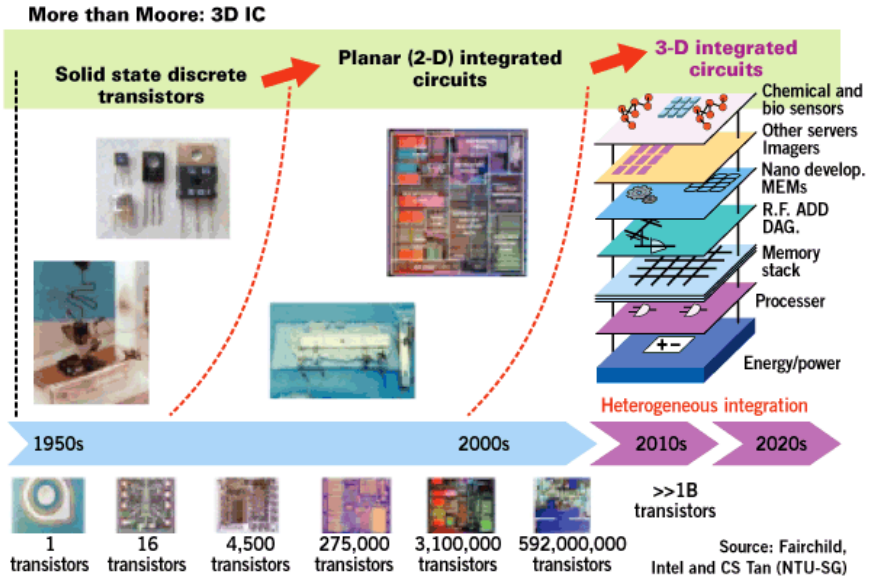


Figure 50: Historical trend in microelectronic device integration. After [213].

Indeed, in a circuit with 2D planar implementation, energetic particles have a relative shallow and unobstructed path to reach the active surface of the silicon chip [214]. Under 3D integration technologies, stacking multiple dies on top of each other suggests that the incident particles need to penetrate through multiple layers of

material before they can strike transistors on the inner layers. Whether the stacked dies have the capability of intercepting particles before they reach deep into the 3D chip and how this could change the soft error rate (SER) across different layers of the 3D chip are largely unknown.

Zhang and Li [214] conducted one of the first studies to evaluate the microarchitecture vulnerability of 3D chips. In this work, they developed an analytical model and a simulation framework to quantify the impact of 3D integration on the microarchitecture soft error rate. Figure 51 (left) shows a cross-section view of the simulated 3D processor. The thickness of each die is around 27 µm with 2 µm spacing between two dies. Making the hypothesis that alpha particles are exclusively emitted from the package and that the circuit SER is proportional to the alpha particle flux, they evaluated the different fluxes reaching the stacked dies (Fig. 51 right). One can deduce from these calculations the existence of an inherent shielding effect of vertical die stacking, capable of reducing the SER of inner layers by up to 90%. The authors concluded that this feature opens opportunities for selectively deploying reliability-hardening SOI techniques to vulnerable layers, which reduces the substrate cost by 75%, compared to a planar processor built on top of SOI wafer.

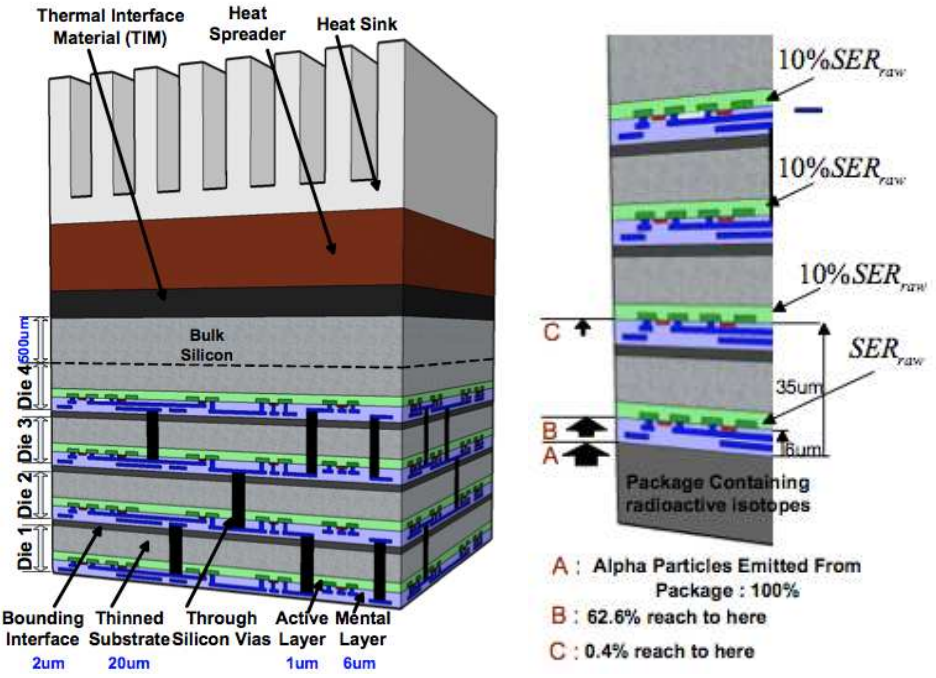


Figure 51.Left: A cross-section view of the simulated 3D processor. Right: Percentage of alpha particles emitted from the contaminated package and reaching active layers on each die. After Zhang and Li [214].

Gouker et al. [215-216] have conducted another recent and very complete study of radiation effects in 3×64 kbit SOI SRAM circuits fabricated using a novel 3D process developed at MIT Lincoln Laboratory (3DIC technologie). In this approach, three fully fabricated 2D circuit wafers have been stacked using standard CMOS fabrication techniques including thin-film planarization, layer alignment and oxide bonding. Micron-scale dense 3D viashave been fabricated to interconnect circuits between tiers. Figure 52 compares the cross-section of a 2D SOI integrated circuit and a 3DIC wafer with three FDSOI CMOS tiers. The 3D-IC has eleven interconnect-metal layers; the SRAM active circuitry is confined within a 20 µm thick layer above the SOI substrate.

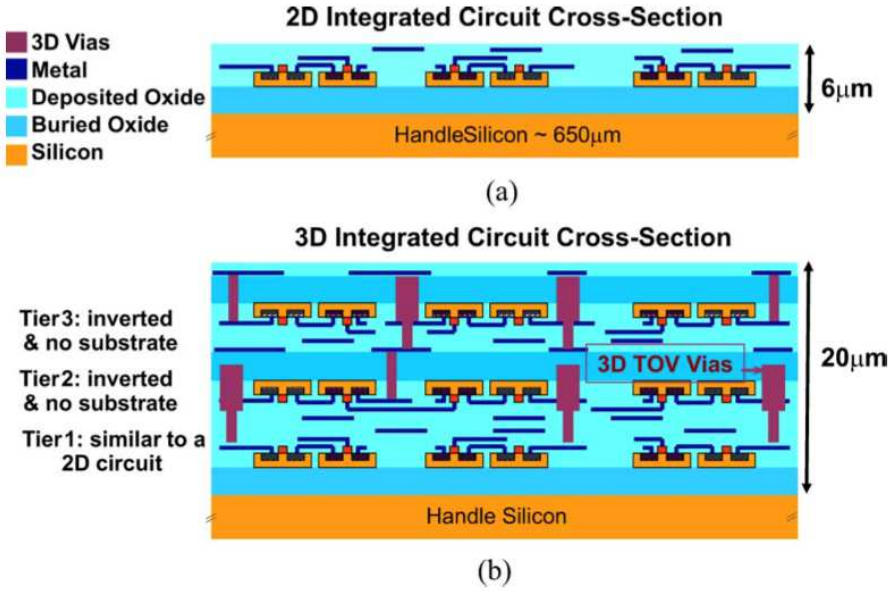


Figure 52.Illustrated cross-section of a) a 2D integrated circuit and b) a 3D IC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D Though Oxide Vias (TOV) interconnecting tiers 1, 2 and 3. After Gouker et al. [215]. © 2011 Institute of Electrical and Electronics Engineers Inc.

In their work, Gouker et al. [215] showed that these 3D SOI SRAMs are tolerant to ionizing radiation induced by 500-MeV protons at least up to 100 krad (Si). Testing with protons with energies between 4.8 and 500MeV and 14-MeV neutrons yielded similar results. The upset cross sections for 3D SOI SRAMs have been found similar for all tiers, and they are also similar to that for single-tier 2D SRAMs. Differences between tiers were directly attributed to variations in the critical dimensions of the sensitive volume defined by the device width, gate length and SOI thickness. Angular effects measured with protons and neutrons were also directly attributed to the change in the particle path length within the sensitive volume. The upset cross section has an in- verse-cosine dependence on the neutron/protons incident angle. No tier-to-tier effects were identified. Monte Carlo simulations confirmed the experimental results. Finally, the authors concluded that radiation hardening design techniques that have been successfully implemented in single-tier 2D circuits will be effective in 3D ICs.

5 Summary

This short-course surveyed the state-of-the-art research works in the domain of single event effects (SEE) related to advanced CMOS technologies. After a brief overview of basic SEE phenomena, we described the radiation environments vs. applications (space, atmospheric and ground level) and the main sources of natural radiation at ground level, including atmospheric radiation and telluric radiation sources. SEE production at silicon level has been also recalled as well as the SEE terminology and the main SEU mechanisms occurring in memories (SBU, MCU) and in digital circuits. We have paid a particular attention to SEE modeling and simulation issues, successively describing device-level and circuit-level modeling approaches and giving an overview on Monte Carlo simulation tools.

The evolving trends for emergent devices and circuits have been presented and discussed in details, starting from the context of the microelectronic area (device and circuit roadmap) and focusing on the scaling effects in current technologies that may impact the SEE sensitivity of circuits. We have successively passed in review the geometric scaling and its implications for soft errors, the ion-track structure versus device dimensions, the confinement of carriers in wells and the related electrical effects, the impact of variability on SEE, the evolution of the critical charge, the increasing sensitivity to background radiation and the low alpha material issue.

Emerging devices and related mechanisms have then been reviewed with a special attention for Silicon-on-Insulator (SOI) technologies, multi-gate devices, bulk and SOI FinFE, multi-gate and multi-channel devices with independent gates, III-V FinFET and Tunnel FET and, finally, junctionless devices. We concluded this short-course with a short focus on SEE in 3D integrated circuits, a "More than Moore" near-term perspective allowing electronic system integration in the third dimension.

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7 References

[1] G.E. Moore, Electronics, vol. 38, p. 19 (1965) ;
see also : http://www.intel.com/research/silicon/mooreslaw.htm

[2] E.P. Gusev, V. Narayanan, and M.M. Frank, “Advanced high-k dielectric stacks with polySi and metal gates: Recent progress and current challenges”, IBM Journal of Research and Development, vol. 50, no. 4/5, pp. 387–410, 2006.

[3] Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, S.-H. Lo, G. Sai-Halasz, R. Viswanathan, H.-J.C. Wann, S. Wind, and H.-S.Wong, “CMOS scaling into the nanometer regime”, Proceedings of IEEE, vol. 85, pp. 486–504, 1997.

[4] M.V. Fischetti and S.E. Laux, “Long-Range Coulomb Interactions in Small Si Devices. Part I: Performance and Reliability”, Journal of Applied Physics, vol. 89, no. 2, pp. 1205–1231, 2001.

[5] ITRS 2012. International Technology Roadmap for Semiconductors. Available online: http://public.itrs.net.

[6] M. Houssa, Fundamental and Technological Aspects of High-k Gate Dielectrics, Institute of Physics, London.

[7] K. Rim, J.L. Hoyt, and J.F. Gibbons, “Transconductance Enhancement in Deep Submicron Strained-Si 12-MOSFETs”, Proceedings of IEDM Technical Digest, pp. 707–710, Washington, USA, Dec. 1998.

[8] W. Haensch, E.J. Nowak, R.H. Dennard, P.M. Solomon, A. Bryant, O.H. Dokumaci, A. Kumar, X. Wang, J.B. Johnson, and M.V. Fischetti, “Silicon CMOS devices beyond scaling”, IBM Journal of Research and Development, vol. 50, no. 4/5, pp. 339-361, 2006.

[9] T. Hiramoto, M. Saitoh, and G. Tsutsui, “Emerging nanoscale Silicon devices taking advantage of nanostructure physics”, IBM Journal of Research and Development, vol. 50, no. 4/5, pp. 411-418, 2006.

[10] P.E. Dodd, “Device Simulation of Charge Collection and Single-Event Upset”, IEEE Trans. Nucl. Sci., vol. 43, no. 2, pp. 561-575, April 1996.

[11] P.E. Dodd and L.W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics”, IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 583–602, Jun. 2003.

[12] P.E. Dodd, “Physics-Based Simulation of Single-Event Effects“, IEEE Trans. Device Mater. Reliab., vol. 5, no. 3, pp. 343-357, Sept. 2005.

[13] R.C. Baumann, “Radiation-Induced Soft Errors in Advanced Semiconductor Technologies”, IEEE Trans. Device Mater. Reliab., vol. 5, no. 3, pp. 305-316, Sept. 2005.

[14] S. Mitra, P. Sanda, and N. Seifert, “Soft Errors: Technology Trends, System Effects and Protection Techniques,” IEEE VLSI Test Symposium, 2008.
[15] P. Roche, “Year-in-Review on radiation-induced Soft Error Rate”, tutorial at IEEE International Reliability Physics Symposium, San Jose, USA, March 2006.
[16] R.D. Schrimpf, D.M. Fleetwood (Editors), Radiation Effects And Soft Errors In Integrated Circuits And Electronic Devices, World Scientific Publishing (2004).
[17] E. Normand, “Single Event Upset at Ground Level”, IEEE Transactions on Nuclear Science, Volume NS-43, N°6, pp. 2742-2750, 1996. See also references therein.
[18] D.F. Heidel, P.W. Marshall, K.A. LaBel, J.R. Schwank, K.P. Rodbell, M.C. Hakey, M.D. Berg, P.E. Dodd, M.R. Friendlich, A.D. Phan, C.M. Seidleck, M.R. Shaneyfelt, and M.A. Xapsos, “Low Energy Proton Single-Event-Upset Test Results on 65 nm SOI SRAM”, IEEE Transactions on Nuclear Science, vol 55, no. 6, pp. 3394-3400, 2008.
[19] E.H. Cannon, M. Cabanas-Holmen, J. Wert, T. Amort, R. Brees, J. Koehn, B. Meaker, and E. Normand, ”Heavy Ion, High-Energy, and Low-Energy Proton SEE Sensitivity of 90-nm RHBD SRAMs”, IEEE Transactions on Nuclear Science, vol. 56, no. 7, pp. 3493-3499, 2010.
[20] J.F. Dicello, C.W. McCabe, J.D. Doss, and M. Paciotti, “The relative efficiency of soft-error induction in 4K static RAMs by muons and pions”, IEEE Transactions on Nuclear Science, vol 30, no. 6, pp. 4613-4616, 1983.
[21] C.J. Gelderloos, R.J. Peterson, M E. Nelson, and J.F. Ziegler, “Pion-Induced Soft Upsets in 16 Mbit DRAM Chips”, IEEE Transactions on Nuclear Science, vol 44, Issue 6, pp. 2237-2242, 1997.
[22] S. Duzellier, D. Falguère, M. Tverskoy, E. Ivanov, R. Dufayel, and M.C. Calvet, “SEU Induced by Pions in Memories From Different Generations”, IEEE Transactions on Nuclear Science, vol 48, no. 6, pp. 1960-1965, 2001.
[23] B.D. Sierawski, M.H. Mendenhall, R.A. Reed, M.A. Clemens, R.A. Weller, R.D. Schrimpf, E.W. Blackmore, M. Trinczek, B. Hitti, J.A. Pellish, R.C. Baumann, S.-J. Wen, R. Wong, and N. Tam, “Muon-Induced Single Event Upsets in Deep-Submicron Technology”, IEEE Trans. Nucl. Sci., vol. 57, no. 6, pp. 3273 - 3278, 2010.
[24] B.D. Sierawski, R.A. Reed, M.H. Mendenhall, R.A. Weller, R.D. Schrimpf, S. Wen, R. Wong, N. Tam, and R.C. Baumann, “Effects of scaling on muon-induced soft errors”, International Reliability Physics Symposium (IRPS 2011), pp. 3C3.1-6.
[25] J.F. Ziegler and H. Puchner, SER – History, Trends and Challenges, Cypress Semiconductor, 2004. See also references therein.
[26] J.L. Autran, D. Munteanu, P. Roche, G. Gasiot, S. Martinie, S. Uznanski, S. Sauze, S. Semikh, E. Yakushev, S. Rozov, P. Loaiza, G. Warot, M. Zampaolo, "Soft-errors induced by terrestrial neutrons and natural alpha-particle emitters in advanced memory circuits at ground level", Microelectronics Reliability, Vol. 50, pp. 1822-1831, 2010.
[27] L.I. Dorman, Cosmic Rays in the Earth’s Atmosphere and Underground, Kluwer Academic Publishers, 2004.
[28] M.S. Gordon, P. Goldhagen, K.P. Rodbell, T.H. Zabel, H.H.K. Tang, J.M. Clem, P. Bailey, "Measurement of the Flux and Energy Spectrum of Cosmic-Ray Induced Neutrons on the Ground", IEEE Trans. Nucl. Sci., Vol. 51, N°6, 2004, pp. 3427-3434.
[29] F. Lei, S. Clucas, C. Dyer, and P. Truscott, “An atmospheric radiation model based on response matrices generated by detailed Monte Carlo Simulations of cosmic ray interactions”, IEEE Trans. Nucl. Sci., vol. 51, pp. 3442-3451, 2004.
[30] F. Lei, A. Hands, S. Clucas, C. Dyer, and P. Truscott, “Improvement to and Validations of the QinetiQ Atmospheric Radiation Model (QARM)”, IEEE Trans. Nucl. Sci., vol. 53, pp. 1851-1858, 2006.
[31] F. Wrobel, J. Gasiot, and F. Saigné, “Hafnium and Uranium Contributions to Soft Error Rate at Ground Level”, IEEE Transactions on Nuclear Science, 2008, Vol. 55, pp. 3141-3145.
[32] G. Adamiec and M. Aitken, “Dose-rate conversion factors: update”, Ancient TL, vol. 16, no. 2, pp. 37-50, 1998.
[33] JEDEC Standard – Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices, JESD89 revision v1.0, 2006.
[34] EIA/JEDEC Standard – Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation, EIA-JESD57, Dec. 1996.
[35] ESCC25100 – Single Event Effects Test Method and Guidelines, ESCC Basic Specification No. 25100, Oct. 2002.

[36] T. Karnik, P. Hazucha, and J. Patel, “Characterization of soft errors caused by single event upsets in CMOS processes,” IEEE Trans. Dependable Secure Comput., vol. 1, no. 2, pp. 128-143, Apr.-Jun. 2004.

[37] T. V. Rajeevakumar, N.C.C. Lu, W.H. Henkels, W. Hwang, R. Franch, “A New Failure Mode of Radiation-Induced Soft Errors in Dynamic Memories”, IEEE Electron Device Lett., vol. 9, pp. 644-646, Dec. 1988.

[38] P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, J. R. Schwank, “Production and propagation of single-event transients in high-speed digital logic ICs”, IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3278-3284, Dec. 2004.

[39] R. C. Baumann, “Single event effects in advanced CMOS Technology,” in Proc. IEEE Nuclear and Space Radiation Effects Conf. (NSREC). Short Course Text, 2005.

[40] S. Buchner and M. Baze, “Single-event transients in fast electronic circuits,” in Proc. IEEE Nuclear and Space Radiation Effects Conf. (NSREC). Short Course Text, 2001.

[41] L.W. Massengill, “SEU modeling and prediction techniques,” in Proc. IEEE Nuclear and Space Radiation Effects Conf. (NSREC). Short Course Text, 1993.

[42] J.M. Benedetto, P.H. Eaton, D.G. Mavis, M. Gadlage, and T. Turflinger, “Variation of digital SET pulse widths and the implications for single event hardening of advanced CMOS processes”, IEEE Trans. Nucl. Sci., vol. 52, pp. 2114–2119, Dec. 2005.

[43] J. Benedetto, P. Eaton, K. Avery, D. Mavis, M. Gadlage, and T. Turflinger, “Heavy ion induced digital single-event transients in deep submicron processes”, IEEE Trans. Nucl. Sci., vol. 51, pp. 3480–3485, Dec. 2004.

[44] P. Eaton, J. Benedetto, D. Mavis, K. Avery, M. Sibley, M. Gadlage, T. Turflinger, “Single event transient pulse width measurements using a variable temporal latch technique”, IEEE Trans. Nucl. Sci., vol. 51, pp. 3365-3368, Dec. 2004.

[45] M.J. Gadlage, R.D. Schrimpf, J.M. Benedetto, P.H. Eaton, D.G. Mavis, M. Sibley, K. Avery, and T.L. Turflinger, “Single event transient pulse widths in digital microcircuits”, IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3285–3290, Dec. 2004.

[46] J.M. Benedetto, P.H. Eaton, D.G. Mavis, M. Gadlage, and T. Turflinger, “Digital Single Event Transient Trends With Technology Node Scaling”, IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3462-3465, Dec. 2006.

[47] B. Narasimham, B.L. Bhuva, W.T. Holman, R.D. Schrimpf, L.W. Massengill, A.F. Witulski, and W.H. Robinson, “The Effect of Negative Feedback on Single Event Transient Propagation in Digital Circuits”, IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3285-3290, Dec. 2006.

[48] V. Ferlet-Cavrois, L.W. Massengill, and P. Gouker, “Single Event Transients in Digital CMOS – A Review”, IEEE Trans. Nucl. Sci., vol. 60, no. 3, pp. 1767–1790, June 2013.

[49] S.E. Diehl, J.E. Vinson, B.D. Shafer, and T.M. Mnich, “Considerations for single event immune VLSI logic”, IEEE Trans. Nucl. Sci., vol. NS-30, no. 6, pp. 4501-4507, Dec. 1983.

[50] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger, “Comparison of error rates in combinational and sequential logic”, IEEE Trans. Nucl. Sci., vol. 44, no. 6, pp. 2209-2216, Dec. 1997.

[51] T. Heijmen, B. Kruseman, R. van Veen, M. Meijer, “Technology Scaling of Critical charges in Storage circuits Based on Cross-Coupled Inverter-Pairs”, in Proc. IEEE Int. Reliability Physics Symp., pp. 675-676, Apr. 2004.

[52] P. Roche and G. Gasiot, “Impacts of Front-End and Middle-End Process Modifications on Terrestrial Soft Error Rate”, IEEE Trans. Device Mater. Reliab., vol. 5, no. 3, pp. 382-396, Sept. 2005.

[53] P. Shivakumar, M. Kistler, S.W. Keckler, D. Burger, L. Alvisi, “Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic”, in Proc. Int. Conf. Dependable Systems and Networks, DSN 2002.

[54] H. Cha and J.H. Patel, “A Logic-Level Model for α-Particle Hits in CMOS Circuits”, in Proc. IEEE Int. Conf. Computer Design, pp. 538-542, Oct. 1993.

[55] P. Liden, P. Dahlgren, R. Johansson, and J. Karlsson, “On Latching Probability of Particle Induced Transients in Combinational Networks”, in Proc. Int. Symp. Fault-Tolerant Computing, pp. 340-349, Jun. 1994.

[56] P. Dahlgren and P. Liden, “A Switch-Level Algorithm for Simulation of Transients in Combinational Logic”, in Proc. IEEE Int. Symp. Fault-Tolerant Computing, pp. 207-216, Jun. 1995.

[57] D. Munteanu and J.L. Autran, “Modeling of digital devices and ICs submitted to transient irradiations”, IEEE Trans. Nucl. Sci., vol. 55, no. 4, pp. 1854-1878, 2008.

[58] S. Selberrer, Analysis and Simulation of Semiconductor Devices, Springer-Verlag, Wien New York, 1984.

[59] M. Lundstrom, Fundamentals of Carrier Transport, Modular Series on Solid State Devices, vol. X, G.W. Neudeck, R.F. Pierret, Editors.
[60] Y. Apanovich, E. Lyumkis, B. Polski, A. Shur, and P. Blakey, “Steady-State and Transient Analysis of Submicron Devices Using Energy Balance and Simplified Hydrodynamic Models”, IEEE Trans. Computer-Aided Integrated Circuits and Systems, vol. 13, no. 6, pp. 702-711, Jun. 1994.
[61] R. Stratton, “Diffusion of Hot and Cold Electrons in Semiconductor Barriers”, Phys. Rev., vol. 126, no. 6, pp. 2002-2013, 1962.
[62] K. Blotekjaer, “Transport Equations for Electron in Two-Valley Semiconductors”, IEEE Trans. Electron Devices, vol. ED-17, no. 1, pp. 38-47, 1970.
[63] C. Jacoboni and L. Reggiani, “The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials”, Rev. Mod. Phys., vol. 55, no. 3, pp. 645–705, July 1983.
[64] M. Fischetti and S. Laux, “Monte Carlo analysis of electron transport in small semiconductor devices including band-structure and space-charge effects”, Phys. Rev. B, vol. 38, no. 14, pp. 9721-9745, 1988.
[65] U. Ravaioli, B. Winstead, C. Wordelman, and A. Kepkep, “Monte-Carlo simulation for ultra-small MOS devices”, Superlattices and Microstructures, vol. 27, no. 2/3, pp. 137-145, 2000.
[66] W. Quade, M. Rudan, and E. Scholl, “Hydrodynamic Simulation of Impact-Ionisation Effects in P-N Junctions”, IEEE Trans. Computer-Aided Design, vol. 10, no. 10, pp. 1287-1294, 1991.
[67] J.R.F. McMacken and S.G. Chamberlain, “An Impact Ionization Model for Two-Carrier Energy-Momentum Simulation”, Simulation of Semiconductor Devices and Processes, vol. 4, pp. 499, 1991.
[68] Synopsys Sentaurus TCAD tools, Available online: http://www.synopsys.com/products/tcad/tcad.html
[69] Athena/Atlas User’s Manual, Silvaco International, Santa Clara, CA, 2004.
[70] P. Roche, “Etude du basculement induit par une particule ionisante dans une mémoire statique en technologie submicronique”, Phd Thesis, 1999 (in French).
[71] Y. Song, K.N. Vu, J.S. Cable, A.A. Witteles, W.A. Kolasinski, R. Koga, J.H. Elder, J.V. Osborn, R.C. Martin, and N.M. Ghoniem, “Experimental and analytical investigation of single event, multiple bit upsets in poly-Silicon load, 64 K × 1 NMOS SRAMs”, IEEE Trans. Nucl. Sci., vol. 35, no. 6, pp. 1673–1677, Dec. 1988.
[72] S.S. Rathod, A.K Saxena, and S. Dasgupta, “Radiation Effects in MOS-based Devices and Circuits: A Review”, IETE Tech. Rev., vol. 28, no. 6, pp. 451-469, 2011.
[73] S. Uznanski, “Single Event Upsets in Sub-65nm CMOS technologies, Monte-Carlo simulations and contribution to understanding of physical mechanisms”, Ph.D. Thesis, edited by LAP LAMBERT Academic Publishing (ISBN-13: 978-3-8465-9551-0), 2011.
[74] K. Mayaram, J.H. Chern, and P. Yang, “Algorithms for transient three dimensional mixed-level circuit and device simulation”, IEEE Trans. Computer-Aided Des. Integr. Circuits Syst., vol. 12, pp. 1726–1733, 1993.
[75] J. G. Rollins and J. Choma Jr., “Mixed-mode pisces-spice coupled circuit and device solver”, IEEE Trans. Computer-Aided Des. Integr. Circuits Syst., vol. 7, pp. 862–867, 1988.
[76] Davinci Three-Dimensional Device Simulation Program Manual, Synopsys, Inc., Mountain View, CA, 2003.
[77] P. Roche, J. M. Palau, K. Belhaddad, G. Bruguier, R. Ecoffet, and J. Gasiot, “SEU response of an entire SRAM cell simulated as one contiguous three dimensional device domain”, IEEE Trans. Nucl. Sci., vol. 45, no. 6, pp. 2534–2543, Dec. 1998.
[78] P. Roche, J.-M. Palau, C. Tavernier, G. Bruguier, R. Ecoffet, and J. Gasiot, “Determination of key parameters for SEU using full cell 3-D SRAM simulations”, IEEE Trans. Nucl. Sci., vol. 46, no. 6, pp. 1354-1362, Dec. 1999.
[79] P.E. Dodd, M.R. Shaneyfelt, K.M. Horn, D.S. Walsh, G.L. Hash, T.A. Hill, B.L. Draper, J.R. Schwank, F.W. Sexton, and P.S. Winokur, “SEU-sensitive volumes in bulk and SOI SRAMs from first-principles calculations and experiments”, IEEE Trans. Nucl. Sci., vol. 48, pp. 1893-1903, Dec. 2001.
[80] R.A. Weller, R.D. Schrimpf, R.A. Reed, M.H. Mendenhall, K.M. Warren, B.D. Sierawski, and L.W. Massengill, “Monte Carlo simulation of Single Evenet Effects”, Short-Course, RADECS 2009.
[81] R.A. Reed, R.A. Weller, A. Akkerman, J. Barak, S. Duzellier, C. Foster, M. Gaillardin, G. Hubert, T. Jordan, I. Jun, S. Koontz, F. Lei, P. McNulty, M.H. Mendenhall, M. Murat, P. Nieminen, P. O’Neil, M. Raine, B. Reddell, F. Saigné, G. Santin, L. Sihver, H.H.K. Tang, P.R. Truscott, and F. Wrobel, “Anthology of the

Development of Radiation Transport Tools as Applied to Single Event Effects", IEEE Trans. Nucl. Sci., vol. 60, no. 3, pp. 1876–1911, June 2013.

[82] H.H.K. Tang, "SEMM-2: A new generation of single-event-effect modeling tools", IBM Journal of Research and Development, vol. 52, no. 3, pp. 233–244, 2008.

[83] F. Wrobel and F. Saigné, "MC-ORACLE: A tool for predicting Soft Error Rate", Computer Physics Communications, vol. 182, pp. 317-321, 2011.

[84] S. Agostinelli et al., "Geant4—a simulation toolkit", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 506, pp.250-303, 2003.

[85] J.L. Autran, S. Semikh, D. Munteanu, S. Serre, G. Gasiot, and P. Roche, "Soft-Error Rate of Advanced SRAM Memories : Modeling and Monte Carlo Simulation, Numerical Simulation - From Theory to Industry", edited by Mykhaylo Andriychuk, ISBN : 978-953-51-0749-1, InTech, pp. 309-336, Sept. 2012. Available online at http://dx.doi.org/10.5772/50111

[86] S. Uznanski, G. Gasiot, P. Roche, C. Tavernier, J-L. Autran, "Single Event Upset and Multiple Cell Upset Modeling in Commercial Bulk 65 nm CMOS SRAMs and Flip-Flops," IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 1876 - 1883, Aug 2010.

[87] S. Uznanski, G. Gasiot, P. Roche, and J.L. Autran, "Combining GEANT4 and TIARA for Neutron Soft Error Rate Prediction of 65 nm Flip-Flops," IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2599 - 2606, Dec 2011.

[88] SRIM software, available online: http://www.srim.org/

[89] Virtual Geometry Model (VGM), available online: http://ivana.home.cern.ch/ivana/VGM.html

[90] ROOT, an object oriented framework for large scale data analysis, available online: http://root.cern.ch

[91] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, R. Mahnkopf, J. Pelka, J.-U. Pfeiffer, A. Rouzaud, M. Tartagni, C. Van Hoof, and J. Wagner, "Towards a "More-than-Moore" roadmap", Report from the CATRENE Scientific Committee, available online http://public.itrs.net.

[92] Y.C. Hung. CMOS Nonlinear Signal Processing Circuits, Advances in Solid State Circuit Technologies, Paul K Chu (Ed.), ISBN: 978-953-307-086-5, InTech, DOI: 10.5772/8630. Available from: http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/cmos-nonlinear-signal-processing-circuits

[93] G. Gasiot, A. Castelnovo, M. Glorieux, F. Abouzeid, S. Clerc, and P. Roche, "Process Variability Effect on Soft Error Rate by Characterization of Large Number of Samples", IEEE Trans. Nucl. Sci., vol. 59, no. 6, pp. 2914-2919, Dec. 2012.

[94] L.W. Massengill, B.L. Bhuva, W.T. Holman, M.L. Alles, T.D. Loveless, "Technology Scaling and Soft Error Reliability", 2012 IEEE Intl. Reliability Physics Symposium (IRPS), pp.3C.1.1-3C.1.7, 2012.

[95] B. Sierawski, "Low-Energy Proton Single Event Upsets in SRAMs", 3rd Annual NEPP Electronic Technology Workshop (ETW), presentation available online at http://nepp.nasa.gov/workshops/etw2012/talks/Tuesday/T12_Sierawski_Low_Energy_Proton_SEE.pdf

[96] P. Roche, "Year-In-Review on SER", tutorial at the International Reliability Physics Symposium (IRPS), Phoenix, 2006.

[97] M. Raine, M. Gaillardin, P. Paillet, O. Duhamel, S. Girard, and A. Bournel, "Experimental Evidence of Large Dispersion of Deposited Energy in Thin Active Layer Devices", IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2664-2672, Dec. 2011.

[98] R.N. Hamm, J.E. Turner, H.A. Wright, and R.H. Ritchie, "Heavy ion track structure in Silicon", IEEE Trans. Nucl. Sci., vol. 26, no. 6, pp. 4892–4895, Dec. 1979.

[99] R.C. Martin, N.M. Ghoniem, Y. Song, and J.S. Cable, "The size effect of ion charge tracks on single event multiple-bit upset", IEEE Trans. Nucl. Sci., vol. 34, no. 6, pp. 1305–1309, 1987.

[100] P. Oldiges, R. Dennard, D. Heidel, B. Klaasen, R. Assaderaghi, and M. Ieong, "Theoretical determination of the temporal and spatial structure of α-particle induced electron-hole pair generation in Silicon", IEEE Trans. Nucl. Sci., vol. 47, no. 6, pp. 2575–2579, Dec. 2000.

[101] M. Raine, "Etude de l' effet de l'énergie des ions lourds sur la sensibilité des composants électroniques", Ph.D. Thesis (in French), 2011, available at : http://tel.archives-ouvertes.fr/docs/00/64/73/28/PDF/VD_RAINE_MELANIE_27092011.pdf

[102] P.E. Dodd, O. Musseau, M.R. Shaneyfelt, F.W. Sexton, C. D'hose, G.L. Hash, M. Martinez, R.A. Loemker, J.-L. Leray, and P.S. Winokur, "Impact of ion energy on single-event upset", IEEE Trans. Nucl. Sci., vol. 45, no. 6, pp. 2483–2491, Dec. 1998.

[103] E.J. Kobetich and R. Katz, "Energy Deposition by Electron Beams and δ Rays", Physical Review, vol. 170, no. 2, pp. 391-396, 1968.

[104] W.J. Stapor and P.T. McDonald, “Practical approach to ion track energy distribution”, J. Appl. Phys., vol. 64, no. 9, pp 4430-4434, 1988.
[105] M.P.R. Waligorski, R.N. Hamm, and R. Katz, “The radial distribution of dose around the path of a heavy ion in liquid water,” Nucl. Tracks Rad. Meas., vol. 11, pp. 309–319, 1986.
[106] O. Fageeha, J. Howard, and R.C. Block, “Distribution of radial energy deposition around the track of energetic particles in silicon,” J. Appl. Phys., vol. 75, no. 5, pp. 2317–2321, 1994.
[107] H. Dussault, J.W. Howard, Jr., R.C. Block, M.R. Pinto, W.J. Stapor, A.R. Knudson, “Numerical simulation of heavy ion charge generation and collection dynamics”, IEEE Trans. Nucl. Sci., vol. 40, no. 6, pp. 1926–1934, Dec. 1993.
[108] ——, “The effects of ion track structure in simulating single event phenomena”, in Proc. Radiation and Effects Components and Systems (RADECS), St. Malo, France, 1993, pp. 509–516.
[109] M. Raine, G. Hubert, M. Gaillardin, L. Artola, P. Paillet, S. Girard, J.-E. Sauvestre, and A. Bournel, " Impact of the Radial Ionization Profile on SEE Prediction for SOI Transistors and SRAMs Beyond the 32-nm Technological Node", IEEE Trans. Nucl. Sci., vol. 58, no. 3, pp. 840-847, June 2011.
[110] K.P. Rodbell, D.F. Heidel, J.A. Pellish, P.W. Marshall, H.H.K. Tang, C.E. Murray, K.A. LaBel, M.S. Gordon, K.G. Stawiasz, J.R. Schwank, M.D. Berg, H.S. Kim, M.R. Friendlich, A.M. Phan, and C.M. Seidleck, “32 and 45 nm Radiation-hardened-by-design (RHBD) SOI latches,” IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2702–2710, Dec. 2011.
[111] D.F. Heidel, P.W. Marshall, J.A. Pellish, K.P. Rodbell, K.A. LaBel, J.R. Schwank, S.E. Rauch, M.C. Hakey, M.D. Berg, C.M. Cas- taneda, P.E. Dodd, M.R. Friendlich, A.D. Phan, C.M. Seidleck, M.R. Shaneyfelt, and M.A. Xapsos, “Single-event upsets and multiple-bit upsets on a 45 nm SOI SRAM,” IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3499–3504, Dec. 2009.
[112] D. Giot, P. Roche, G. Gasiot, J.L. Autran, and R. Harboe-Sørensen, “Heavy Ion Testing and 3-D Simulations of Multiple Cell Upset in 65 nm Standard SRAMs,” IEEE Trans. Nucl. Sci., vol. 55, no. 4, pp. 2048–2054, Aug. 2008.
[113] J.L. Autran, S. Serre, D. Munteanu, S. Martinie, S. Semikh, S. Sauze, S. Uznanski, G. Gasiot, and P. Roche, “Real-Time Soft-Error Testing of 40nm SRAMs”, 2012 IEEE Intl. Reliability Physics Symposium (IRPS), pp. 3C.5.1-3C.5.9, 2012.
[114] F. Arnaud, L. Pinzelli, C. Gallon, M. Rafik, P. Mora, and F. Bœuf, "Challenges and opportunity in performance, variability and reliability in sub-45 nm CMOS technologies”, Microelectronics Reliability, vol. 51, pp. 1508–1514, 2011.
[115] S.M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, “An Analytical Model for Soft Error Critical Charge of Nanometric SRAMs”, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 9, pp. 1187-1195, Sept. 2009.
[116] P. Hazucha and C. Svensson, “Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate”, IEEE Trans. Nucl. Sci., vol. 47, vo. 6, pp. 2586-2594, Dec. 2000.
[117] Y.Z. Xu et al., “Process impact on SRAM alpha-particle SEU performance,”in Proc. IEEE Int. Rel. Phys. Symp., Phoenix, AZ, pp. 294–299, 2004.
[118] B. Zhang, A. Arapostathis, S. Nassif, and M. Orshansky, “Analytical modeling of SRAM dynamic stability,” in Proc. IEEE/ACM Int. Conf. on Computer-Aided Design, San Jose, CA, pp. 315–322, 2006.
[119] E.L. Petersen, P. Shapiro, J.H. Adams, Jr., E.A. Burke, “Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices,” IEEE Trans. Nuclear Science, vol.29, no.6, pp. 2055-2063, Dec. 1982.
[120] N. Seifert , B. Gill , J.A. Pellish , P.W. Marshall and K.A. LaBel "The susceptibility of 45 and 32 nm bulk CMOS latches to low-energy protons", IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp.2711 -2718, 2011.
[121] K. Rodbell, D. Heidel, H. Tang, M. Gordon, P. Oldiges, and C. Murray, “Low-energy proton-induced single-event-upsets in 65 nm node, silicon-on-insulator, latches and memory cells,” IEEE Trans. Nucl. Sci., vol. 54, no. 6, pp. 2474–2479, Dec. 2007.
[122] B.D. Sierawski, J.A. Pellish, R.A. Reed, R.D. Schrimpf, K.M. Warren, R.A. Weller, M.H. Mendenhall, J.D. Black, J.A.D. Tipton, M.A. Xapsos, R.C. Baumann, D. Xiaowei, M.J. Campola, M.R. Friendlich, H.S. Kim, A.M. Phan, and C.M. Seidleck, “Impact of low-energy proton induced upsets on test methods and rate predictions,” IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3085–3092, Dec. 2009.
[123] J. Insoo, M.A. Xapsos, S.R. Messenger, E.A. Burke, R.J. Walters, G.P. Summers, and T. Jordan, “Proton nonionizing energy loss (NIEL) for device applications,” IEEE Trans. Nucl. Sci., vol. 50, no. 6, pp. 1924–1928, Dec. 2003.

[124] H. Puchner, J. Tausch, and R. Koga, “Proton-Induced Single Event Upsets in 90nm Technology High Performance SRAM Memories”, Radiation Effects Data workshop, NSREC July 2011.
[125] J.F. Ziegler and W.A. Lanford, “Effect of cosmic rays on computer memories”. Science, Vol. 206, November 1979.
[126] T. Suzuki, D.F. Measday, J.P. Roalsvig, “Total nuclear capture rates for negative muons”. Physical Review C, Vol. 35 No. 6, June 1987.
[127] S.E. Sobottka and E.L. Wills, “Energy spectrum of charged particles emitted following muon capture in ^{28}Si”, Physical Review Letters, vol. 20, no. 12, March 1968.
[128] R.M. Sundelin and R.M. Edelstein, “Neutron Asymmetries and Energy Spectra from Muon Capture in Si, S, and Ca”, Phys. Rev. C 7, pp. 1037–1060, 1973.
[129] R.M. Sundelin, R.M. Edelstein, S. Suzuki and K. Takahashi, “Spectrum of neutrons from muon capture in silicon, sulfur, and calcium”. Physical Review Letters, vol. 20, no. 21, May 1968.
[130] B. Macdonald, J.A. Diaz, S.N. Kaplan, and R.V. Pyle, “Neutrons from Negative-Muon Capture”, Phys. Rev., vol. 139, pp. B1253–B1263,1965.
[131] Y.G. Budyashov, V.G. Zinov, A.D. Konin, A.I. Mukhin, and A.M. Chatrchyan, “Charged Particles from the Capture of Negative Muons by the Nuclei 28Si, 32S, 40Ca, and 64Cu”. Soviet Journal of Experimental and Theoretical Physics, vol. 33, p. 11, 1971.
[132] A. Wyttenbach, P. Baertschi, S. Bajo, J. Hadermann, K. Junker, S. Katcoff, E.A. Hermes, and H.S. Pruys, “Probabilities of muon induced nuclear reactions involving charged particle emission”, Nuclear Physics A, vol. 294, no. 3, pp. 278–292, 1978.
[133] S. Serre, S. Semikh, J.L. Autran, D. Munteanu, G. Gasiot, and P. Roche, "Effects of Low Energy Muons on Electronics: Physical Insights and Geant4 Simulation", Proceedings of the 2012 Conference on Radiation and its Effects on Components and Circuits (RADECS), 24-28 September 2012, IEEE Xplore Digital Library.
[134] F. Wrobel, J. Gasiot, F. Saigné, and A.D. Touboul, “Effects of atmospheric neutrons and natural contamination on advanced microelectronic memories”, Appl. Phys. Lett., vol. 93, 064105, 2008.
[135] S. Martinie, J.L. Autran, S. Sauze, D. Munteanu, S. Uznanski, P. Roche, and G. Gasiot, “Underground Experiment and Modeling of Alpha Emitters Induced Soft-Error Rate in CMOS 65 nm SRAM,” IEEE Trans. Nucl. Sci., vol. 59, no. 4, pp. 1048–1053, Aug. 2012.
[136] Brett Clark, “The Distribution and Transport of Alpha Activity in Tin”, White paper Honeywell International Inc., 2012. Available at: http://www.honeywell-radlo.com
[137] http://www.honeywell-radlo.com/soft-errors
[138] J.P. Colinge, Silicon-On-Insulator technology: materials to VLSI, 2nd Ed., Kluwer Academic Publishers, 1997.
[139] D. Munteanu, D. Weiser, S. Cristoloveanu, O. Faynot, J.L. Pelloie, and J.G. Fossum, “Generation-Recombination Transient Effects in Partially Depleted SOI Transistors: Systematic Experiments and Simulations”, IEEE Trans. Electron Devices, vol. 45, no. 8, pp. 1678-1683, 1998.
[140] D. Munteanu and A.M. Ionescu, “Modeling of Drain Current Overshoot and Recombination Lifetime Extraction in Floating-Body Submicron SOI MOSFETs”, IEEE Trans. Electron Devices, vol. 49, no. 7, pp. 1198-1205, 2002.
[141] L.W. Massengill, D.V. Kerns, S.E. Kerns and M.L. Alles, “Single-Event Charge Enhancement in SOI Devices”, IEEE Electron Device Lett.., vol. EDL-11. pp. 98-99, February 1990.
[142] O. Musseau, J.L. Leray, V. Ferlet-Cavrois, Y.M. Coic, and B. Giffard, “SEU in SOI SRAMS - a static model”, IEEE Trans. Nucl. Sci., vol. NS-41, no. 3, pp. 607-612, 1994.
[143] V. Ferlet-Cavrois, C. Marcandella, G. Giraud, G. Gasiot, T. Colladant, O. Musseau, C. Fenouillet, J. du Port de Pontcharra, “Characterization of the parasitic bipolar amplification in SOI technologies submitted to transient irradiation”, IEEE Trans. Nucl. Sci., vol. 49, no. 3, pp. 1456-1461, June 2002.
[144] J.R. Schwank, V. Ferlet-Cavrois, M.R. Shaneyfelt, P. Paillet, and P.E. Dodd, “Radiation effects in SOI technologies”, IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 522–538, Jun. 2003.
[145] V. Ferlet-Cavrois, G. Vizkelethy, P. Paillet, A. Torres, J.R. Schwank, M.R. Shaneyfelt, J. Baggio, J. du Port de Pontcharra, and L. Tosti, “Charge enhancement effect in NMOS bulk transistors induced by heavy ion irradiation—Comparison with SOI”, IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3255–3262, Dec. 2004.

[146] O. Musseau, V. Ferlet-Cavrois, J.L. Pelloie, S. Buchner, D. McMorrow, and A.B. Campbell, “Laser probing of bipolar amplification in 0.25-µm MOS/SOI transistors”, IEEE Trans. Nucl. Sci., no. 6, pp. 2196–2203, Dec. 2000.

[147] L.R. Hite, H. Lu, T.W. Houston, D.S. Hurta, and W.E. Bailey, “An SEU resistant 256 K SOI SRAM”, IEEE Trans. Nucl. Sci., vol. 39, pp. 2121–2125, Dec. 1992.

[148] S.E. Kerns, L.W. Massengill, D.V. Kerns Jr, J.M L. Alles, T.W. Houston, H. Lu, and L.R. Hite, “Model for CMOS/SOI single-event vulnerability”, IEEE Trans. Nucl. Sci., vol. 36, pp. 2305–2310, Dec. 1989.

[149] V. Ferlet-Cavrois, P. Paillet, D. McMorrow, A. Torres, M. Gaillardin, J.S. Melinger, A.R. Knudson, A.B. Campbell, J.R. Schwank, G. Vizkelethy, M.R. Shaneyfelt, K. Hirose, O. Faynot, C. Jahan, and L. Tosti, “Direct Measurement of Transient Pulses Induced by Laser Irradiation in Deca-Nanometer SOI Devices”, IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2104-2113, Dec. 2005.

[150] V. Ferlet-Cavrois, G. Gasiot, C. Marcandella, C. D’Hose, O. Flament, O. Faynot, J. du Port de Pontcharra, and C. Raynaud, “Insights on the Transient Response of Fully and Partially Depleted SOI Technologies Under Heavy-Ion and Dose-Rate Irradiations”, IEEE Trans. Nucl. Sci., vol. 49, no. 6, pp. 2948-2956, Dec. 2002.

[151] C. Brisset, P. Dollfus, O. Musseau, J.L. Leray, and P. Hesto, “Theoretical study of SEU’s in 0.25-pm fully-depleted CMOS/SOI technology,” IEEE Trans. Nucl. Sci., vol. 41, no. 6, pp. 2297-2303, 1994.

[152] V. Ferlet-Cavrois, “Comportement des technologies SOI sous irradiations”, HDR report, 2004 (in French).

[153] D. Munteanu, V. Ferlet-Cavrois, J.L. Autran, P. Paillet, J. Baggio, O. Faynot, C. Jahan, and L. Tosti, “Investigation of Quantum Effects in Ultra-Thin Body Single- and Double-Gate Devices Submitted to Heavy Ion Irradiation”, IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3363-3371, Dec. 2006.

[154] P. Paillet, M. Gaillardin, V. Ferlet-Cavrois, A. Torres, O. Faynot, C. Jahan, L. Tosti, and S. Cristoloveanu, “Total Ionizing Dose Effects on Deca-nanometer FD SOI Devices”, IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2345-2352, Dec. 2005.

[155] O. Musseau, "Single-Event-Effects in SOI technologies and devices", IEEE Trans. Nucl. Sci., vol. 43, no. 2, p. 603, April 1996.

[156] M. Gaillardin, P. Paillet, V. Ferlet-Cavrois, J. Baggio, D. McMorrow, O. Faynot, C. Jahan, L. Tosti, and S. Cristoloveanu, “Transient radiation response of single- and multiple-gate FD SOI transistors,” IEEE Trans. Nucl. Sci., vol. 54, no. 6, pp. 2355–2362, Dec. 2007.

[157] D.G. Mavis and P.H. Eaton, “Soft error rate mitigation techniques for modern microcircuits”, in Proc. IEEE Int. Reliability Physics Symp., pp. 216-225, 2002.

[158] J.T. Park and J.P. Colinge, “Multiple-gate SOI MOSFETs: device design guidelines”, IEEE Trans. Electron Devices, vol. 49, no. 12, pp. 2222-2229, Dec. 2002.

[159] D.J. Frank, S.E. Laux, and M.V. Fischetti, “Monte Carlo simulation of a 30nm dual-gate MOSFET: How short can Si go?“, in Int. Electron Devices Meeting Tech. Dig., pp. 553-556, Dec. 1992.

[160] S. Harrison, P. Coronel, F. Leverd, R. Cerutti, R. Palla, D. Delille, S. Borel, S. Descombes, D. Lenoble, A. Talbot, A. Villaret, S. Monfray, P. Mazoyer, J. Bustos, H. Brut, A. Cros, D. Munteanu, J.L. Autran, and T. Skotnicki, “Highly performant double gate MOSFET realized with SON process”, in Int. Electron Devices Meeting Tech. Dig., pp. 449-452, Dec. 2004.

[161] K.W. Guarini, P.M. Solomon, Y. Zhang, K.K. Chan, E.C. Jones, G.M. Cohen, A. Krasnoperova, M. Ronay, O. Dokumaci, J.J. Bucchignano, C. Cabral Jr., C. Lavoie, V. Ku, D.C. Boyd, K.S. Petrarca, I.V. Babich, J. Treichler, P.M. Kozlowski, J.S. Newbury, C.P. D'Emic, R.M. Sicina, and H. Wong, “Triple-self-aligned, planar double-gate MOSFETs: Devices and circuits”, in Int. Electron Devices Meeting Tech. Dig., pp. 425-428, Dec. 2001.

[162] Y. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T. King, J. Bokor, and C. Hu, “Sub-20nm CMOS FinFET technologies”, in Int. Electron Devices Meeting Tech. Dig., pp. 421-424, Dec. 2001.

[163] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K. Lee, B.A. Rainey, D. Fried, P. Cottrell, H.P. Wong, M. Ieong, W. Haensch, “Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation”, in Int. Electron Devices Meeting Tech. Dig., pp. 247-250, Dec. 2002.

[164] J.T. Park, J.P. Colinge, and C.H. Diaz, "Pi-Gate SOI MOSFET", IEEE Electon Device Lett., vol. 22, no.8, pp. 405-406, 2001.

[165] F. Yang, H. Chen, F. Chen, C. Huang, C. Chang, H. Chiu, C. Lee, C. Chen, H. Huang, C. Chen, H. Tao, Y. Yeo, M. Liang, and C. Hu, “25nm CMOS Omega FETs”, in Int. Electron Devices Meeting Tech. Dig., pp. 255-258, Dec. 2002.

[166] Z. Jiao and C.A.T. Salama, “A fully depleted Δ-channel SOI nMOSFET”, in Proc. Electrochem. Soc. 2001–3, pp. 403–408, 2001.

[167] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, “A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET,” in Int. Electron Devices Meeting Tech. Dig., pp. 833–836, Dec. 1989.

[168] J.P. Colinge, M.H. Gao, A. Romano-Rodríguez, H. Maes, and C. Claeys, “Silicon-on-insulator “Gate-all-around device””, in Int. Electron Devices Meeting Tech. Dig., pp. 595-598, Dec. 1990.

[169] D. Jiménez, B. Iniguez, J. Suné, L.F. Marsal, J. Pallarès, J. Roig, and D. Flores, “Continuous Analytic I–V Model for Surrounding-Gate MOSFETs”, IEEE Electron Device Lett., vol. 25, no. 8, pp. 571-573, Aug. 2004.

[170] J.-W. Yang and J.G. Fossum, “On the feasibility of nanoscale triple-gate CMOS transistors,” IEEE Trans. Electron Devices, vol. 52, no. 6, pp. 1159–1164, Jun. 2005.

[171] D. Munteanu, J.L. Autran, V. Ferlet-Cavrois, P. Paillet, J. Baggio, and K. Castellani, “3-D Quantum Numerical Simulation of Single-Event Transients in Multiple-Gate Nanowire MOSFETs”, IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 994-1001, Aug. 2007.

[172] T. Ernst, C. Dupré, C. Isheden, E. Bernard, R. Ritzenthaler, V. Maffini-Alvaro, J.-C. Barbé, F. De Crecy, A.Toffoli, C. Vizioz, S. Borel, F. Andrieu, V. Delaye, D. Lafond, G. Rabillé, J.-M. Hartmann, M. Rivoire, B. Guillaumot, A. Suhm, P. Rivallin, O. Faynot, G. Ghibaudo, and S. Deleonibus, “Novel 3D integration process for highly scalable Nano-Beam stacked-channels GAA (NBG) FinFETs with HfO2/TiN gate stack”, in Int. Electron Devices Meeting Tech. Dig., pp. 997-1000, Dec. 2006.

[173] E. Bernard, T. Ernst, B. Guillaumot, N. Vulliet, X. Garros, V. Maffini-Alvaro, F. Andrieu, V. Barral, F. Allain, A. Toffoli, V. Vidal, V. Delaye, C. Vizioz, Y. Campidelli, O. Kermarrec, J.M. Hartmann, S. Borel, O. Faynot, A. Souifi, P. Coronel, T. Skotnicki, and S. Deleonibus, “Impact of the gate stack on the electrical performances of 3D Multi-Channel MOSFET (MCFET) on SOI”, in Proc. ESSDERC., pp. 147-150, Sept. 2007.

[174] Y. Taur and TH. Ning, Fundamentals of Modern VLSI Devices. Cambridge, UK: Cambridge Univ. Press, 1998.

[175] N. Seifert, B. Gill, S. Jahinuzzaman, J. Basile, V. Ambrose, Q. Shi, R. Allmon, and A. Bramnik, “Heavy-Ion-Induced Current Transients in Bulk and SOI FinFETs”, IEEE Trans. Nucl. Sci., vol. 59, no. 6, pp. 2666 - 2673, Dec. 2012.

[176] X. Huang, W.-C. Lee, D.H.L. Chang, J. Boker, T.J. King, V. Subramanian, and C. Hu, “Sub 50 nm P channel FinFETs,” IEEE Trans. Electron. Devices, vol. 48, no. 5, pp. 880–886, May 2001.

[177] E.J. Nowak, I. Aller, T. Ludwig, K. Kim, R.V. Joshi, C.-T. Chung, K. Bernstein, and R. Puri, “Turning silicon on its edge,” IEEE Circuits Devices Mag., vol. 20, no. 1, pp. 20–31, Jan./Feb. 2004.

[178] C.R. Manoj, M. Nagpal, D. Varghese, and V.R. Rao, “Device Design and Optimization Considerations for Bulk FinFETs”, IEEE Trans. Electron. Devices, vol. 55, no. 2, pp. 609–615, Feb. 2008.

[179] F. El-Mamouni, E.X. Zhang, R.D. Schrimpf, R.D. Reed, K.F. Galloway, D. McMorrow, E. Simoen, C. Claeys, S. Cristoloveanu, and W. Xiong, “Pulsed laser-induced transient currents in bulk and silicon-on-insulator FinFETs,” in Proc. IRPS, 2011, pp. 882–885.

[180] T. Chiarella, L. Witters, A. Mercha, C. Kerner, M. Rakowski, C. Ortolland, L.Å. Ragnarsson, B. Parvais, A. De Keersgieter, S. Kubicek, A. Redolfi, C. Vrancken, S. Brus, A. Lauwers, P. Absil, S. Biesemans, and T. Hoffmann, “Benchmarking SOI and bulk FinFET alternatives for planar CMOS scaling succession,” Solid-State Electron., vol. 54, no. 9, pp. 855–860, Sep. 2010.

[181] F. El-Mamouni, E.X. Zhang, N.D. Pate, N. Hooten, R.D. Schrimpf, R.A. Reed, K.F. Galloway, D. McMorrow, J. Warner, E. Simoen, C. Claeys, A. Griffoni, D. Linten, and G. Vizkelethy, “Laser- and heavy ion-induced charge collection in bulk FinFETs,” IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2563–2569, Dec. 2011.

[182] F. El-Mamouni, E.X. Zhang, D.R. Ball, B. Sierawski, M.P. King, R.D. Schrimpf, R.A. Reed, M.L. Alles, D.M. Fleetwood, D. Linten, E. Simoen, and G. Vizkelethy, “Heavy-Ion-Induced Current Transients in Bulk and SOI FinFETs,” IEEE Trans. Nucl. Sci., vol. 59, no. 6, pp. 2674–2681, Dec. 2012.

[183] D.R. Ball, M.L. Alles, R.D. Schrimpf, and S. Cristoloveanu, “Comparing single event upset sensitivity of bulk vs. SOI based FinFET SRAM cells using TCAD simulations,” in Proc. IEEE Int. SOI Conf., pp. 1–2, 2010.

[184] J.-W. Yang and J.G. Fossum, “On the feasibility of nanoscale triple-gate CMOS transistors,” IEEE Trans. Electron Devices, vol. 52, no. 6, pp. 1159–1164, Jun. 2005.
[185] M. Masahara, Y. Liu, K. Sakamoto, K. Endo, T. Matsukawa, K. Ishii, T. Sekigawa, H. Yamauchi, H. Tanoue, S. Kanemaru, H. Koike, and E. Suzuki, “Demonstration, Analysis, and Device Design Considerations for Independent DG MOSFETs”, IEEE Trans. Electron Devices, vol. 52, no. 9, pp. 2046-2051, Sept. 2005.
[186] G. Pei and E.C. Kan, “Independently Driven DG MOSFETs for Mixed-Signal Circuits: Part I—Quasi-Static and Nonquasi-Static Channel Coupling”, IEEE Trans. Electron. Devices, vol. 51, no. 12, pp. 2086-2093, Dec. 2004.
[187] J.L. Autran and D. Munteanu, “Simulation of electron transport in nanoscale independent-gate DG devices using a full 2D Green’s function approach”, J. Comput. Theoretical Nanosci., vol. 5, pp. 1120–1127, 2008.
[188] L. Mathew, Y. Du, A.V. Thean, M. Sadd, A. Vandooren, C. Parker, T. Stephens, R. Mora, R. Rai, M. Zavala, D. Sing, S. Kalpat, J. Hughes, R. Shimer, S. Jallepalli, G. Workman, W. Zhang, J.G. Fossum, B.E. White, B.Y. Nguyen, and J. Mogab, “CMOS vertical Multiple Independent Gate Field Effect Transistor (MIGFET)”, in Proc. IEEE Int. SOI Conf., pp. 187–189, Oct. 2004.
[189] M. Moreau, D. Munteanu, and J.L. Autran, “Simulation Analysis of Quantum Confinement and Short-Channel Effects in Independent Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistors”, Jpn. J. App. Phys., vol. 47, pp. 7013-7018, 2008.
[190] W. Zhang, J.G. Fossum, L. Mathew, and Y. Du, “Physical Insights Regarding Design and Performance of Independent-Gate FinFETs”, IEEE Trans. Electron. Devices, vol. 52, no. 10, pp. 2198-2206, Oct. 2005.
[191] D. Munteanu and J.L. Autran, “3-D Simulation Analysis of Bipolar Amplification in Planar Double-Gate and FinFET with Independent Gates”, IEEE Trans. Nucl. Sci., vol. 56, no. 4, pp. 2083-2090, Aug. 2009.
[192] D. Munteanu and J.L. Autran, “Simulation Analysis of Bipolar Amplification in Independent-Gate FinFET and Multi-Channel NWFET Submitted to Heavy-Ion Irradiation”, IEEE Trans. Nucl. Sci., vol. 59, no. 6, pp. 3249-3257, Dec. 2012.
[193] K.C. Saraswat et al., in : IEDM 06 Proceedings, 2006, p. 1.
[194] D. McMorrow, T.R. Weatherford, S. Buchner, A.R. Knudson, J.S. Melinger, L.H. Tran, and A.B. Campbell, “Single-event phenomena in GaAs devices and circuits,” IEEE Trans. Nucl. Sci., vol. 43, no. 2, pp. 628–644, Apr. 1996.
[195] B.D. Weaver, D. McMorrow, and L.M. Cohn, “Radiation effects in III-V semiconductor electronics,” Int. J. High-Speed Electron. Syst., vol. 13, pp. 293–326, 2003.
[196] D. McMorrow, J.B. Boos, A.R. Knudson, W.T. Lotshaw, D. Park, J.S. Melinger, B. R. Bennett, A. Torres, V. Ferlet-Cavrois, J.-E. Sauvestre, C. D’Hose, and O. Flament, “Transient response of III–V field-effect transistors to heavy-ion irradiation,” IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3324–3331, Dec. 2004.
[197] P.E. Dodd, M.R. Shaneyfelt, J.R. Schwank, and J.A. Felix, “Transient response of III–V field-effect transistors to heavy-ion irradiation,” IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 1747-1763, Aug. 2010.
[198] W. Choi, B. Park, J. Lee, and T. Liu, “Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,” IEEE Electron Device Lett., vol. 28, no. 8, pp. 743–745, Aug. 2007.
[199] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallet, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu, and S. Datta, “Experimental demonstration of 100 nm channel length In0.53Ga0.47As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications,” in IEDM Tech. Dig., pp. 1–3, Dec. 2009.
[200] P. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weiss, D. Schmitt-Landsiedel, and W. Hansch, “Complementary tunneling transistor for low-power applications,” Solid State Electron., vol. 48, no. 12, pp. 2281–2286, Dec. 2004.
[201] J.L. Padilla, F. Gámiz, and A. Godoy, “Impact of Quantum Confinement on Gate Threshold Voltage and Subthreshold Swings in Double-Gate Tunnel FETs,” IEEE Trans. Electron. Devices, vol. 59, no. 12, pp. 3205-3211, Dec. 2012.
[202] A. Verhulst, B. Soree, D. Leonelli, W. Vandenberghe, and G. Groeseneken, “Modeling the single-gate, double-gate and gate-all-around tunnel fieldeffect transistor,” J. Appl. Phys., vol. 107, no. 2, pp. 024518-1–024518-8, Jan. 2010.
[203] Y. Khatami and K. Banerjee, “Steep subthreshold slope n- and p-type tunnel-FET devices for low-power and energy-efficient digital circuits,” IEEE Trans. Electron Devices, vol. 56, no. 11, pp. 2752–2761, Nov. 2009.
[204] K. Jeon, W.-Y. Loh, P. Patel, Y. Kang, J. Oh, A. Bowonder, C. Park, C. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J. Liu, and C. Hu, “Si tunnel transistors

with a novel silicided source and 46 mv/dec swing," in Proc. VLSIT Symp., pp. 121–122, Jun. 2010.

[205] H. Liu, M. Cotter, S. Datta, and V. Narayanan, "Technology Assessment of Si and III-V FinFETs and III-V Tunnel FETs from Soft Error Rate Perspective", in Proceedings of IEDM Technical Digest, pp. 577-580, 2012.

[206] C.-W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, and J.P. Colinge, "Junctionless multigate field-effect transistor," Applied Physics Letters, vol. 94, p. 053511, 2009.

[207] J.P. Colinge, C.-W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," Nature Nanotechnology, vol. 5, 2010.

[208] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N.D. Akhavan, P. Razavi, and J.P. Colinge, "High Temperature Performance of Silicon Junctionless MOSFETs," IEEE Trans. Electron Devices, vol. 53, no. 3, pp. 620–625, 2010.

[209] A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J.P. Colinge, "Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines", in Proc. European Solid State Device Research Conf. (ESSDERC), pp. 357-360, 2010.

[210] C-Y. Chen, J-T. Lin, M-H. Chiang, and K. Kim, "High-Performance Ultra-Low Power Junctionless Nanowire FET on SOI Substrate in Subthreshold Logic Application", in Proc. SOI Conference, 2010.

[211] J.P. Colinge, C.-W. Lee, I. Ferain, N.D. Akhavan, R. Yan, P. Razavi, R. Yu, A.N. Nazarov, and R.T. Doria, "Reduced electric field in junctionless transistors," Applied Physics Letters, vol. 96, p. 073510, 2009.

[212] D. Munteanu and J.L. Autran, "3-D Numerical Simulation of Bipolar Amplification in Junctionless Double-Gate MOSFETs Under Heavy-Ion Irradiation", IEEE Trans. Nucl. Sci., vol. 59, no. 4, pp. 773-780, Aug. 2012.

[213] http://www.electroiq.com/articles/sst/2013/01/iedm-2012-the-pivotal-point-for-monolithic-3d-ics.html

[214] W. Zhang and T. Li, "Microarchitecture Soft Error Vulnerability Characterization and Mitigation under 3D Integration Technology", 41st IEEE/ACM International Symposium on Microarchitecture (MICRO-41), pp. 435-446, 2008.

[215] P.M. Gouker, B. Tyrrell, R.D'Onofrio, P. Wyatt, T. Soares, W. Hu, C. Chen, J.R. Schwank, M.R. Shaneyfelt, E.W. Blackmore, K. Delikat, M. Nelson, P. McMarr, H. Hughes, J.R. Ahlbin, S. Weeden-Wright, and R. Schrimpf, "Radiation Effects in 3D Integrated SOI SRAM Circuits", IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2845-2854, Dec. 2011.

[216] P.M. Gouker, B. Tyrrell, M. Renzi, C. Chen, P. Wyatt, J.R. Ahlbin, S. Weeden-Wright, N.M. Atkinson, N.J. Gaspard, B.L. Bhuva, L.W. Massengill, E. Zhang, R. Schrimpf, R.A. Weller, M.P. King, and M.J. Gadlage, "SET Characterization in Logic Circuits Fabricated in a 3DIC Technology", IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2555-2562, Dec. 2011.