Modeling and Simulation of Single-Event Effects in Digital Devices and ICs

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INTRODUCTION

The phenomenal success of CMOS technology, and, by consequence, the progress of the information technology, can be attributed without any doubt to the scaling of the MOS transistor, which has been pushed during more than thirty years to increasingly levels of integration and performances. Then, MOSFETs have been fabricated always smaller, denser, faster and cheaper in order to provide ever more powerful products for digital electronics. Recently, the scaling rate has accelerated, and the MOSFET gate length is now less than 40 nm, with devices entering into the nanometer world (Fig. 1) [1]-[2]. The so-called "bulk" MOSFET is the basic and historical key-device of microelectronics: its dimensions have been reduced more than ~10^3 times during the three past decades. However, the bulk MOSFET scaling has recently encountered significant limitations, mainly related to the gate oxide (SiO_2) leakage currents [3]-[4], the large increase of parasitic short channel effects and the dramatic mobility reduction [5]-[6] due to highly doped Silicon substrates precisely used to reduce these short channel effects. Technological solutions have been proposed in order to continue to use the "bulk solution" until the 45 nm ITRS node. Most of these solutions envisage the introduction of high-permittivity gate dielectric stacks (to reduce the gate leakage, [4], [7]-[8]), midgap metal gate (to suppress the Silicon gate polydepletion-induced parasitic capacitances) and strained Silicon channel (to increase carrier mobility, [9]-[11]). However, in parallel to these efforts, alternative solutions to replace the conventional bulk MOSFET architecture have been proposed and studied in the recent literature. These options are numerous (Fig. 2) and can be classified in general according to three main directions: (i) the use of new materials in the continuity of the "bulk solution", allowing increasingly MOSFET performances due to their dielectric properties (permittivity), electrostatic immunity (SOI materials), mechanical (strain), or transport (mobility) properties; (ii) the complete change

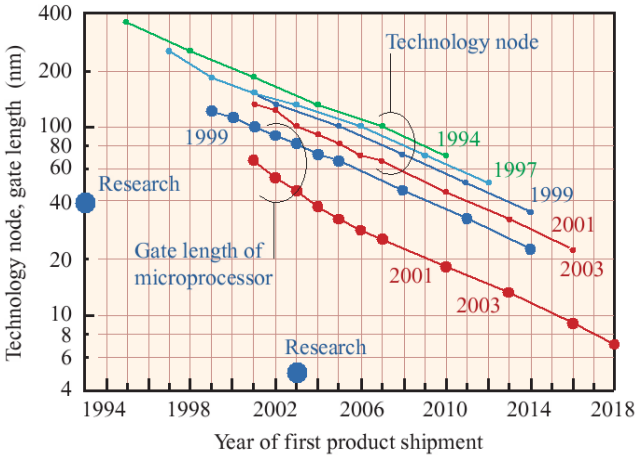

Fig. 1. Prediction of gate length of MOSFETs in high performance (HP) microprocessors by ITRS [1]. Technology nodes predicted by the 1994–2003 versions of ITRS and gate lengths predicted by the 1999–2003 versions of ITRS are plotted. The predictions of the 2001 version and the 2003 version are the same. Shortest devices reported in research are also shown from 1993 and 2003 bibliography. After Hiramoto *et al*. [2]. © 2006 IBM, reproduced with permission.

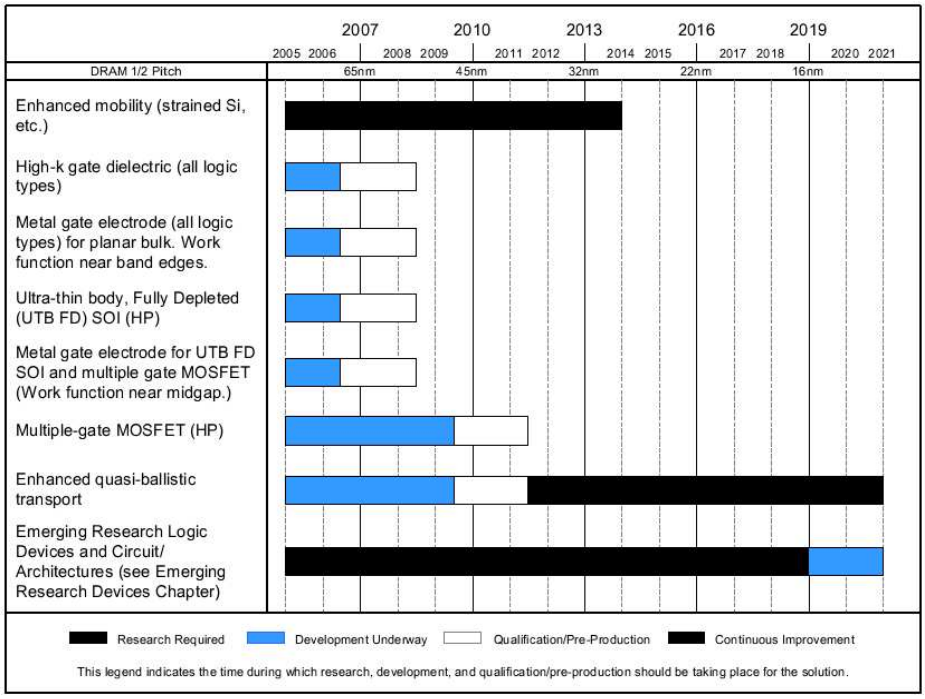

Fig. 2. Potential solutions for the continuation of the MOSFETs scaling (high-performance logic applications). After the 2006 edition of the International Technology Roadmap for Semiconductors (ITRS, [1]). © 2006 International Technology Roadmap for Semiconductors, reproduced with permission.

of the device architecture (e.g. multiple-gate devices, Silicon nanowires MOSFET) allowing better electrostatic control, and, as a result, intrinsic channels with higher mobilities and currents; (iii) the exploitation of certain new physical phenomena that appear at the nanometer scale, such as quantum transport, substrate orientation or modifications of the material band structure in devices/wires with nanometer dimensions [2], [12].

As the MOSFET is scaling down, the sensitivity of the integrated circuits to radiation coming from the natural space or present in the terrestrial environment has been found to seriously increase [13]-[16]. In particular, ultra-scaled memory ICs are more sensitive to single-event-upset (SEU) and digital devices are more subjected to digital single-event transient (DSETs). Single-event-effects (SEE) are the result of the interaction of highly energetic particles, such as protons, neutrons, alpha particles, or heavy ions, with sensitive regions of a microelectronic device or circuit. These SEE may perturb the device/circuit operation (e.g., reverse or flip the data state of a memory cell, latch, flip-flop, etc.) or definitively damage the circuit (e.g. gate oxide rupture, destructive latch-up events).

Modeling and simulating the effects of ionizing radiation has long been used for better understanding the radiation effects on the operation of devices and circuits. In the last two decades, due to substantial progress in simulation codes and computer performances which reduce computation times, simulation reached an increased interest. Due to its predictive capability, simulation offers the possibility to reduce radiation experiments and to test hypothetical devices or conditions, which are not feasible (or not easily measurable) by experiments. Physically-based numerical simulation at device-level presently becomes an indispensable tool for the analysis of new phenomena specific to short-channel devices (non-stationary effects, quantum confinement, quantum transport), and for the study of radiation effects in new device architectures (such as multiple-gate, Silicon nanowire MOSFET), for which experimental investigation is

still limited. In these cases, numerical simulation is an ideal investigation tool for providing physical insights and predicting the operation of future devices expected for the end of the roadmap.

A complete description of the modeling and simulation of SEE, including the history and the evolution of this research domain, have been presented in the reference survey papers by Dodd [13]-[15] and Baumann [16]. In this short-course we would like to review the current status of modeling of digital devices and circuits, with a special emphasis on the current challenges concerning the physical modeling of the ultra-scaled devices and new device architectures. The short-course is organized as follows. The next sections of this introductive part present the classification and the terminology used in the paper, as well as the basic mechanisms of SEE, their impact on microelectronic devices, and the interest of modeling and simulation. The introduction of the short-course is followed by two parts: part I discusses device modeling approaches and part II deals with circuit level simulation. In part I, we firstly present the transport models used in device simulation (drift-diffusion, hydrodynamic, Monte-Carlo and quantum approaches). Next the emerging physical phenomena in ultra-short MOSFETs are described in detail and the methods envisaged for taking them into account in device modeling are presented. Two other important issues of SEE simulation are discussed: the necessity of considering a 3-D (real space) domain approach for device-level simulation and a realistic ion track as input in simulation. Several examples of simulation at device level are given at the end of part I, based on our recent results on fully-depleted SOI and multiple-gate devices. In part II, we briefly survey the different circuit-level modeling approaches (circuit-level simulation, Mixed-Mode, 3-D simulation of full circuit) of single-event effects in integrated circuits. The SEU in advanced SRAM and SEE mechanisms in logic circuits are reminded. Digital single-event transient (DSETs) production and propagation in sequential and combinational logic, as well as the soft error rate trends with scaling are particularly addressed. Three masking effects (logical, temporal and electrical masking) which naturally reduce the soft-error rate in combinational logic are reminded. A few typical examples of simulation in SRAM (bulk and SOI Double-Gate) and logic circuits (flip-flop, inverter chains) are finally presented and discussed to illustrate these circuit-level approaches.

A. Classification and terminology

As defined by the JEDEC standard JESD89A [17], single-event effects (SEE) indicate any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike. Single-event effects include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET), single-event burnout (SEB) and single-event gate rupture (SEGR). The soft error rate (SER) indicates the rate at which soft errors occur. We precise in the following the most important terms and related definitions:

- *Soft error, device*: An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell. As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process. Soft errors can be generated from SEU, SEFI, MBU, MCU, and or SET. The term SER has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc. are typically used by the avionics, space and military electronics communities. Historically, the term “soft error” was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term “single event upset” was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).

- *Single-event upset (SEU)*: A soft error caused by the transient signal induced by a single energetic particle strike.

• *Single-event upset (SEU) cross-section*: The number of events per unit fluence. For device SEU cross-section, the dimensions are sensitive area per device. For bit SEU cross-section, the dimensions are area per bit.

• *Single-event upset (SEU) rate*: The rate at which single event upsets occur.

• *Single event transient (SET)*: A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by a single energetic particle strike.

• *Single-event latch-up (SEL)*: An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality. SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation. An example of SEL in a CMOS device is when the passage of a single particle induces the creation of parasitic bipolar (p-n p-n) shorting of power to ground.

• *Single-event gate rupture (SEGR)*: Total or partial damage of the dielectric gate material due to an avalanche breakdown.

In addition to the previous terminology, we mention here, for memory, the following definitions:

• *Multiple-cell upset (MCU)*: A single event that induces several cell upsets in an integrated circuit to fail at one time. The struck cells are adjacent (contrary to the corresponding error bits that are not always adjacent).

• *Multiple-bit upset (MBU)*: A multiple-cell upset in which two or more error bits occur in the same word data (an MBU cannot be corrected by a simple single-bit error-code correction).

• *Single-event functional interrupt (SEFI)*: A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single event burnout (SEB). Note that a SEFI is often associated with an upset in a control bit or register.

• *Hard error*: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events). The error is "hard" because the data is lost and the component or device no longer functions properly even after power reset and re-initialization. The generic term single-event hard error (SEHE) is also used in literature.

• *Linear energy transfer (LET)* of a particle: The energy lost by unit of length, which is expressed here in MeV cm^2/mg (1 pC/μm $\approx$ 100 MeV cm^2/mg in Silicon). The magnitude of the disturbance an incident particle causes primarily depends on the LET of that particle.

B. Basic mechanisms of single-event effects on microelectronic devices

The physical mechanisms related to the production of SEE in microelectronic devices consist in three main successive steps: (1) the charge deposition by the energetic particle striking the sensitive region, (2) the transport of the released charge into the device and (3) the charge collection in the sensitive region of the device. Fig. 3 schematically shows these successive steps in the case of the passage of a high-energy ion through a reverse-biased n^+/p junction. In the following we succinctly describe these different mechanisms, for a detailed presentation we invite the reader to consult ref. [13]-[16].

Charge deposition (or generation): When an energetic charged particle strikes the device, an electrical charge along the particle track can be deposited by one of the following mechanisms: direct ionization by

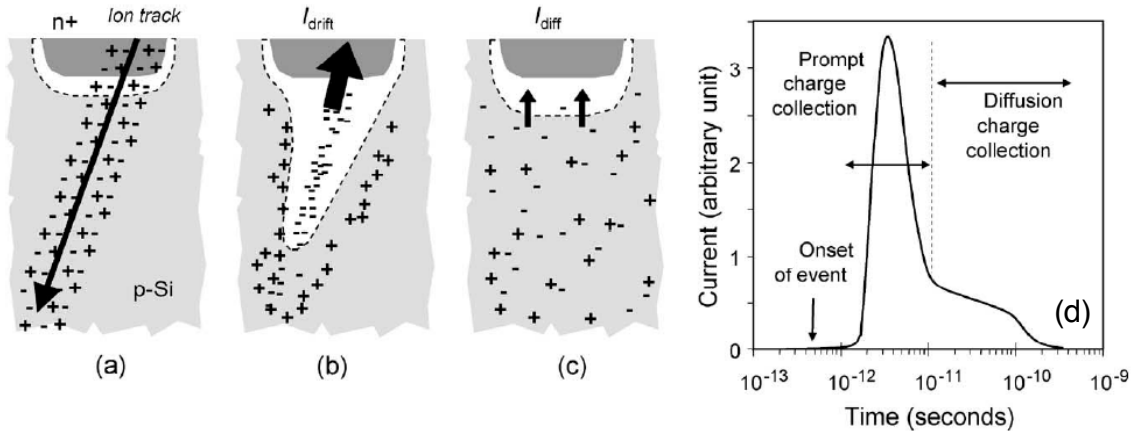

Fig. 3. Charge generation, transport and collections phases in a reverse-biased junction and the resultant current pulse caused by the passage of a high-energy ion. After Baumann [16]. © 2005 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

the interaction with the material or indirect ionization, by secondary particles issued from nuclear reactions with the atoms of the struck material. Direct ionization typically characterizes heavy ions ($Z \geq 2$) of the space environment. They interact with the target material mainly by inelastic interactions and transmit a large amount of energy to the electrons of the struck atoms. These electrons produce a cascade of secondary electrons which thermalize and create electron-hole pairs along the particle path [Fig. 3(a)].

In a semiconductor or insulator, a large amount of the deposited energy is thus converted into electron-hole pairs, the remaining energy being converted into heat and a very small quantity in atoms displacement. It was experimentally shown that the energy necessary for the creation of an electron-hole pair depends on the material bandgap. In a Silicon substrate, one electron-hole pair is produced for every 3.6 eV of energy lost by the ion. Other particles, such as the neutrons of the terrestrial environment, do not interact directly with target material since they do not ionize the matter on their passage. However, these particles should not be neglected, because they can produce SEE due to their probability of nuclear reaction with the atoms of materials which compose the microelectronic devices. This mechanism is called indirect ionization. The products resulting from a nuclear reaction can deposit energy along their traces, in the same manner as that of direct ionization. Since the creation of the column of electron-hole pairs of these secondary particles is similar to that of ions, the same models and concepts can be used.

Charge transport: When a charge column is created in the semiconductor by an ionizing particle, the released carriers are quickly transported and collected by elementary structures (e.g. p-n junctions). The transport of charge relies on two main mechanisms [Figs. 3(b) and 3(c)]: the charge drift in regions with an electric field and the charge diffusion in neutral zones. The deposited charges can also recombine with other mobile carriers existing in the lattice.

Charge collection: The charges transported in the device induce a parasitic current transient [Fig. 3(d)], which could induce disturbances in the device and associated circuits. The devices most sensitive to ionizing particle strikes are generally devices containing reversely-biased p-n junctions, because the strong electric field existing in the depletion region of the p-n junction allows a very efficient collection of the deposited charge. The effects of ionizing radiation are different according to the intensity of the current transient, as well as the number of impacted circuit nodes. If the current is sufficiently important, it can induce a permanent damage on gate insulators (gate rupture, SEGR) or the latch-up (SEL) of the device. In usual low power circuits, the transient current may generally induce only an eventual change of the logical state (cell upset).

C. Interest of modeling and simulation

The continuous reduction of the feature size in microelectronics requires increasingly complicated and time-consuming manufacturing processes. At the same time, the fabrication of emerging devices with alternative architecture, such as multiple-gate or Silicon nanowire transistors, is very expensive and not yet mature. This renders difficult and expensive a systematical experimental investigation of the radiation effects on these new ultra-scaled devices. Since computers are today considerably cheaper resources, simulation is becoming an indispensable tool for the device engineer, not only for the device optimization, but also for specific studies such as the device sensitivity when submitted to ionizing radiation. In addition, as the MOSFET dimensions are reduced in the nanometer scale, the device behavior becomes increasingly complicated while new physical phenomena specific to the ultra-short channels appear (such as quantum confinement, quasi-ballistic transport or parameter fluctuations). It becomes now mandatory to understand the mechanisms of these emerging phenomena and their impact on the device sensitivity to radiation. Then, the growing interest in modeling and simulation of single-event effects in microelectronic devices relies on unique capabilities, summarized below:

(i) Simulation provides useful insights into device operation since all internal physical quantities that can not be measured on real devices are available as outputs in simulation. Several quantities in real devices are sometimes too small or too fast and cannot be measured.

(ii) "What if" studies, which are not feasible by experiment, can be performed in simulation [15].

(iii) The predictive capability of simulation studies makes possible the reduction of the radiation experiments [15].

(iv) Emerging phenomena appearing in ultra-scaled devices can be taken into account in simulation. The influence of these phenomena on the sensitivity to radiations of future device can be investigated in simulation studies.

(v) Simulation offers the possibility to test hypothetical devices which have not yet been manufactured.

PART I. DIGITAL DEVICES MODELING

In this first part, we survey the different device modeling approaches of single-event effects at device-level. We begin by presenting the transport models used in device simulation (drift-diffusion, hydrodynamic, Monte-Carlo and quantum models). Next, the emerging physical phenomena in ultra-short MOSFETs (quantum confinement, ballistic transport, tunneling) are described in detail and the methods envisaged for taking them into account in simulation at device level are presented. Two other important issues of SEE simulation are discussed: (i) the necessity of using 3-D codes for the simulation of the actual devices and (ii) the ion track structure to be used as input in simulation. Several examples of simulation at device level are given at the end of this part I, based on our recent results on fully-depleted SOI and multiple-gate devices.

I. DEVICE MODELING APPROACHES

A. Transport models

Historically, the first models used in carrier transport simulation describe the physical phenomena taking place in the device as functions of the electric field, even if these phenomena depend on carrier energy [18]. This is possible when considering that carrier energy is in permanent balance with the electric field. Carrier transport in MOSFET devices is mainly due to electrostatic potential gradients

and/or gradients of carrier concentration [18]. The current density in a biased device is then usually modeled by the sum of a conduction component (drift) and a diffusion component, as follows (for electrons):

$$J_n = q\mu_n nE + qD_n \nabla n \quad (1)$$

where μ_n is the carrier mobility, D_n is the thermal diffusion coefficient, E is the electric field and n is the electron density. D_n and μ_n depend on material and electric field and are connected by the Einstein's equation:

$$D_n = \mu_n \frac{kT_L}{q} \quad (2)$$

with T_L the lattice temperature. Similar equations are considered for holes (see the paragraph "Drift-Diffusion" below).

This traditional description of electronic transport constitutes the "Drift Diffusion" (DD) model, the basic model used in CMOS devices simulation [18]-[19]. This modeling level is generally adapted for long devices, with either weak or strong electric fields (except for the modeling of impact ionization; see below in this paragraph). When the device feature size is reduced, the electronic transport becomes qualitatively different from the traditional transport model since the average carrier velocity does not depend on the local electric field. Average carrier velocity is a function of the carrier energy which depends on the variations in time and space of the electric field. In short devices steep variations of electric field take place in the active area of the devices. Then, non-stationary phenomena (such as velocity overshoot [20]-[23]) occur following these rapid spatial or temporal changes of high electric fields. In small devices, non-stationary phenomena play an important role and may dominate the device operation. Since DD model neglects non-stationary effects, new advanced transport models become mandatory for accurate transport simulation in ultra-short devices [24]-[29].

A second important issue is related to impact ionization phenomenon, particularly relevant to the operation of Silicon-on-Insulator (SOI) MOSFET with partially-depleted films. The impact ionization is an energy threshold phenomenon which directly depends on the carrier energy. The physical mechanism of impact ionization consists in the generation of electron-hole pairs in the device regions where a strong electric field exists (like in the vicinity of the drain regions). An electron with a sufficient energy in the conduction band yields its energy to an electron of the valence band. This last electron then jumps in the conduction band and leaves a hole in the valence band. It thus results a carrier multiplication in the device and the energy threshold necessary for the phenomenon release is roughly the semiconductor bandgap energy. In the case of MOSFET devices, the impact ionization phenomenon becomes important for device operation at high drain biases. The electrons generated by impact ionization go into the channel and amplify the drain current. The holes are pushed back towards the substrate and are then evacuated or not, depending on the type of device. In bulk MOSFETs they are collected by the substrate electrode and create a substrate current. In partially depleted SOI MOSFETs, the existence of the buried oxide prevents the hole evacuation by the substrate electrode; they generally accumulate in the neutral region (body without external contact) of the Silicon film, and increase the body potential leading to drain current kink phenomenon. Modeling approaches of impact ionization based on the only electric field (such as in the traditional "Drift-Diffusion" model) causes important quantitative and qualitative errors [30]; in particular an over-estimation of the impact ionization rate is observed even for long devices. An energy dependent advanced model is then mandatory for a more accurate modeling of the impact ionization phenomenon [31].

A large majority of the advanced models used in physics and engineering for the description of carrier transport is based on the solution of the semi-classical approach of the Boltzmann Transport Equation (BTE). The most accurate approach is the numerical solving of the BTE by the Monte Carlo

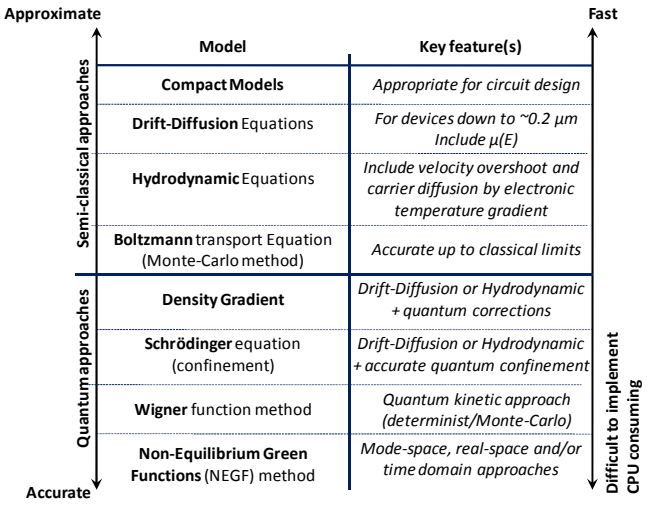

Fig. 4. Illustration of the hierarchy of transport models. Adapted from Vasileska and Goodnick [35].

(MC) method [20], [32]-[33]. Although very accurate results and valuable insights are obtained with this method, MC approach is not routinely used for simulation studies due to considerably time-consuming simulation. An intermediate modeling level relies on hydrodynamic (HD) and energy-transport model (such as Energy Balance) [24]-[29]. These models are obtained from determinist solutions of the BTE and provide a more accurate description of the carrier transport than the DD model.

However, the hydrodynamic model fails in the ballistic limit [34]. One therefore needs to move downward to the quantum transport area in which, different approaches have been developed such as the quantum hydrodynamics model, the quantum Monte-Carlo, the Wigner-Boltzmann approach and Green's function approach. The latter is the most exact, but at the same time the most difficult of all in terms of physical understanding and computational burden [35].

Figure 4 illustrates the various levels of approximation describing charge transport in semiconductor devices. This hierarchical classification highlights the order of increasing level of model accuracy and complexity. In this figure, the transport models range from the one-dimensional compact or analytical modeling used in circuit-level simulation (top) to the exact numerical quantum-mechanical solution given by the Non Equilibrium Green's Function (NEGF) method (bottom) [35]. In the following we succinctly present the different numerical transport modeling approaches; the compact and analytical models will be discussed in part II.

Drift-Diffusion: The drift-diffusion (DD) model was for many years the standard level of solid-state device modeling, mainly due to its simple concept and short simulation times. This approach is appropriate for devices with large feature lengths. This model considers that carrier energy does not exceed the thermal energy and carrier mobility is only a local function of the electric field (mobility does not depend on carrier energy). As noted before, these assumptions are acceptable as long as the electric field changes slowly in the active area, as is the case for long devices.

Most of the simulation software packages for MOSFETs [36]-[38] are based on the solution of the basic semiconductor equations consisting of Poisson's equation coupled with DD model. The simulation code initially solves the Poisson's equation:

$$\nabla(\varepsilon_{Si} \vec{\nabla} \varphi) = -\rho \tag{3}$$

where ρ is the charge density, φ is the electrostatic potential and ε_{Si} is the Silicon permittivity. The DD transport model is described by the following continuity equations:

$$\nabla \vec{J}_n = qR + q\frac{\partial n}{\partial t} \tag{4}$$

$$\nabla \vec{J}_p = -qR - q\frac{\partial p}{\partial t} \tag{5}$$

where R is the generation-recombination rate. Electron and hole current densities are given by:

$$J_n = -q\mu_n n\nabla\varphi + qD_n\nabla n \tag{6}$$

$$J_p = q\mu_p p\nabla\varphi - qD_p\nabla p \tag{7}$$

In equations (6)-(7) the first term of the right-hand side is the drift component and the second term represents the diffusion component (which gives the name Drift-Diffusion to this model). These equations are discretized and solved on a meshed domain using finite-difference or finite-element techniques.

The DD model considers that carriers gain maximum energy instantaneously balanced with the electric field [19]. Then, non-stationary effects (velocity overshoot and carrier transport by thermal diffusion processes associated with electronic temperature gradients) specific to short devices are neglected in DD model, as well as the dependence of impact ionization on the carrier energy. However, DD model is able to assimilate models describing quantum-mechanical confinement effects in short-channel MOSFETs (see next paragraph).

Hydrodynamic model: In reality, the carrier energy does not immediately respond to changes in electric field. Mobility and diffusion coefficients are tensor quantities that depend on several parameters besides electric field [39]. In nano-MOSFETs, the high internal electric fields result in large carrier densities causing substantial electron heating. The hydrodynamic model, obtained by taking the first three moments of the Boltzmann Transport Equation (BTE), represents the carrier transport effects in short devices more accurately than the DD model. The hydrodynamic model is a macroscopic approximation to the BTE taking into account the relaxation effects of energy and momentum. In this model, the propagation of electrons in a semiconductor is treated as the flow of a charged, thermally conducting gas subjected to an electric field. This model removes several limiting assumptions of DD: the carrier energy can exceed the thermal energy and all physical parameters are energy-dependent. The current density and the energy flow are modeled in HD model by the following equations (given here for electrons [37]):

$$\vec{J}_n = q\mu_n\left[-n\vec{\nabla}\varphi + \frac{kT_n}{q}\vec{\nabla}n + \frac{k}{q}(1+\xi_n)n\vec{\nabla}T_n\right] \tag{8}$$

$$div\vec{S}_n = -\vec{J}_n\vec{\nabla}\varphi - \frac{3k}{2}\frac{\partial}{\partial t}(nT_n) - W_n \tag{9}$$

$$\vec{S}_n = -K_n\vec{\nabla}T_n - \frac{k\Delta_n}{q}\vec{J}_nT_n \tag{10}$$

where T_n is the electron temperature, ξ_n is a model coefficient, $\vec{S}_n$ is the energy flow, W_n is the energy density loss rate, K_n is the thermal conductivity and:

$$\Delta_n = \frac{5}{2} + \xi_n \tag{11}$$

while the energy density loss W_n is given by:

$$W_n = \frac{3}{2}n\frac{k(T_n - T_L)}{\tau_{rel}} + \frac{3}{2}kT_nR_{SRH} + E_g(G_n - R_n{}^A) \tag{12}$$

where τ_{rel} is the energy relaxation time, R_{SRH} is the SRH recombination rate, G_n is the impact ionization rate, $R_n{}^A$ is the Auger recombination rate, E_g is the Silicon bandgap. Similar equations are used for holes. Usually, the mobility μ_n is modeled as a decreasing function of energy (because the scattering rate increases with the energy of the particle). Finally, the continuity equations given by (4) and (5) complete the system of equations of the HD model.

Equations (8) to (12) are derived using the following simplifying assumptions:

(i) The temperature tensor reduces to a scalar.

(ii) Closure of the hierarchy of moments in BTE is done by relating the heat flux Q of the electron gas to the electron temperature T_n through the equation $Q = -K_n \nabla Tn$, where the thermal conductivity K_n is given by the Wiedmann–Franz law:

$$K_n = qn\mu_n \left(\frac{k}{q}\right)^2 \Delta_n T_n \tag{13}$$

(iii) The relaxation time approximation is used for modeling the effects of collisions on momentum and energy of the electrons.

The advantage of the HD model over the DD model for transport simulation in short devices can be understood by analyzing Eq. (9), called the "energy-balance equation". The left-hand side of this equation represents the variation of energy flow in space. On the right-hand side, the first term is related to the energy absorbed by the electrons from the electric field. The second term is a representation of the energy supplied by the electrons to the lattice by collisions with optical phonons. Finally, the third term gives the loss of energy through carrier recombination processes. Thus, the equation implies that the spatial variation of energy flow equals the sum-total of heat flow and transported energy. The applicability of the hydrodynamic model in MOSFETs with short channels is justified since in "hot" areas where the electron temperature is high, it predicts a greater diffusion than DD model, due to the finite value of the energy relaxation time [39]. As a result, the average energy and the electron temperature are higher in the regions of strong electric fields compared to their equilibrium values. Moreover, the existing thermoelectric field [the term $\nabla(kT_n/q)$ in Eq. (8)] produces a driving force which makes possible the electron flow from hotter towards colder regions (carrier transport by thermal diffusion processes associated with electronic temperature gradients).

Velocity overshoot phenomenon is the immediate consequence of the finite time needed before the carrier energy reaches equilibrium with the electric field. This phenomenon is primarily due to the non-equivalence of electron momentum and energy relaxation times. The hydrodynamic model is able to correctly predict velocity overshoot, which is not the case of DD model, as previously stated. The velocity overshoot phenomenon can be easily evidenced from the HD model [39]. If one considers a one-dimensional case where the electric field increases in the direction of motion of the particle, the result of the energy balance equation is that the average energy is less than the energy value corresponding to the local electric field under homogeneous conditions. Since mobility is a decreasing function of energy, this means that the velocity given by HD model is stronger than the velocity obtained by DD model, which is based on a mobility that depends on the local electric field.

Direct solution of the Boltzmann Transport Equation (BTE) by Monte Carlo method [20], [32]-[33], [35]. The most accurate approach used in physics and engineering for the description of carrier transport is the Monte Carlo (MC) method. The resolution of the BTE by the Monte Carlo method provides more accurate results than the energy transport models (hydrodynamic), since it does not require simplifying assumptions. The principle of this method is to simulate the free particle motion (referred to as the free flight) terminated by instantaneous random scattering events in the semiconductor. The simulation algorithm is succinctly explained in the following. Carriers are represented like particles with a mass and an electric charge. Firstly, free flight times are randomly generated for each particle. In this phase of simulation all physical quantities characterizing the particles (drift velocity, energy, position) are calculated. In a second phase, a scattering mechanism is randomly chosen according to the scattering probabilities of all the possible scattering mechanisms. The scattering changes the final energy and the momentum of the particle. At the end of this second phase one knows the new quantities related to each particle. Then the procedure is repeated and the particles are subjected to the same succession of physical

phenomena (free flight time ended by a scattering mechanism). Sampling the particle motion at various times throughout the simulation allows for the statistical estimation of physically interesting quantities such as the single particle distribution function, the average drift velocity in the presence of an applied electric field, the average energy of the particles, etc. By simulating an ensemble of particles, representative of the physical system of interest, the non-stationary time-dependent evolution of the electron and hole distributions under the influence of a time-dependent driving force may be simulated.

MC simulation has been used in the past for simulating radiation-induced charge collection [40]-[41] and SEU in short-channel SOI MOSFETs [42]-[43]. Although this method provides the most accurate simulation of short-channel MOSFET, its use is limited because of enormous computational burden. This major drawback prevents Monte-Carlo method to be intensively used for simulation studies of single-event effects.

Quantum transport approaches. As device dimensions continue to shrink, the channel lengths (widths and/or thicknesses) are approaching the characteristic wavelength of particles (for example, the de Broglie wavelength at the Fermi energy) and quantum effects are expected to be increasingly important. Quantum confinement was known to exist in inversion layers of past MOSFET technologies, but it has been considered to have only a second-order influence on the overall device behavior. However, quantum effects (related to both carrier confinement and quantum ballistic transport) may dominate the device operation in actual and future technologies: for example, it is expected that direct source-to-drain tunneling should be a serious limiting physical phenomena for the future device scaling (typically below 6-8 nm channel length). The transport models presented above (Drift-Diffusion, Energy Transport, Monte-Carlo) do not have predictive capability for simulating quantum transport in ultra-small structures; quantum transport tools are presently needed for accurate description of nano-device operation. Different approaches have been developed, one of the most exact being the solving of the Schrödinger equation with open boundary conditions, as performed using the Non-Equilibrium Green's Function (NEGF) formalism. At the same time this approach is the most difficult, in terms of physical complexity and computational burden. Other models have been proposed, generally based on quantum corrections to classical tools, such as Density-Gradient model [44]-[49] (based on a quantum-mechanical correction applied to the carrier density within the Drift-Diffusion or the hydrodynamic model), the inclusion of quantum corrections into Monte-Carlo simulators (using the effective potential method [35]), the Wigner approach (which can be applied in the frame of Monte-Carlo simulation [50] or of a deterministic code). These approaches are less CPU time consuming (except the Monte-Carlo approach), but less accurate. For example, the Wigner function approach does not allow one to simultaneously consider correlations in space and time, both of which are expected to be

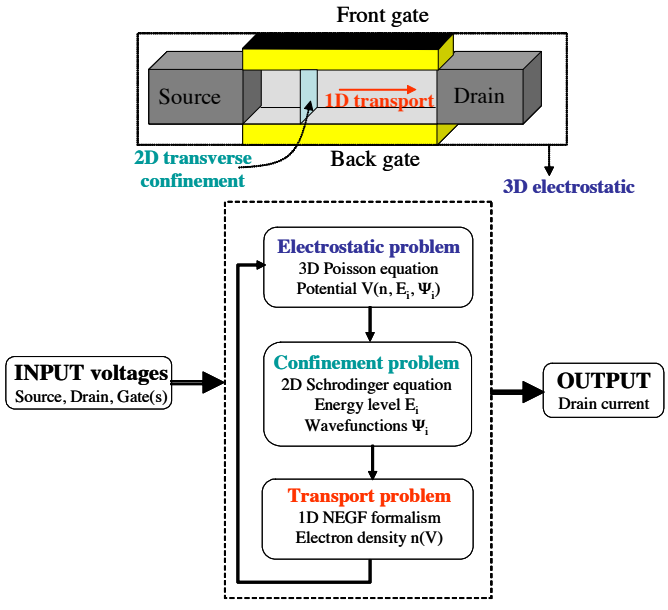

Fig. 5. Schematic representation of a nanowire MOS transistor and typical flowchart of a numerical code illustrating the different problems to solve in the NEGF-calculation of the output drain current (mode-space approach).

important in nano-scale devices. The NEGF formalism [51]-[54] has the capability to treat quantum-mechanical confinement, reflection and tunneling at the same time. The most developed approaches in literature currently consider effective mass band-structure approximation and mode-space approach: the 1-D (respect. 2-D) Schrödinger equation is solved self-consistently with 2-D (respect. 3-D) Poisson equation in the perpendicular direction(s) to the transport direction (with closed boundary conditions to take into account carrier confinement), and carrier transport from source-to-drain is treated in one-dimension using the NEGF formalism (with open boundary conditions). Fig. 5 shows the general algorithm of a NEGF-based code developed in [53]-[54] for simulating multiple-gate devices. This approach is sufficiently accurate for simulating the pure ballistic transport (without scattering) in the channel [55], which gives the highest limit of the device drain current. However, it has been shown that actual and future ultra-short devices will certainly work in a quasi-ballistic regime, where the effects of scattering cannot be neglected. Then, the inclusion of elastic scattering effects due to impurities and interface roughness has to be considered. The NEGF approach offers the additional capability to take into account scattering by using the so-called "Bütiker probe" method [56]: this approach provides a quantum mechanical description of carrier transport and phase randomizing interactions for simulating nanoscale MOSFETs. Recent NEGF developments also consider the use of more sophisticated tight-binding Hamiltonian to take into account the "real" band-structure of the Silicon nanowire playing the role of the conduction channel in nanowire MOSFETs. Finally, NEGF formalism appears well-adapted to treat the carrier transport in real-space with 2-D or 3-D dimensions, as opposed to the mode-space (1-D) approach. In this sense, the Green's function formalism is certainly one of the most promising way for the future developments of new generations of quantum transport simulations tools tackling with atomic scale issues, multi-dimensional and time-dependent approaches. The rigorous time-dependent treatment of the passage of an ionizing particle through a nanodevice with the NEGF method is presently an open theoretical and numerical problem. This simulation challenge is certainly a key-issue for predicting radiation effects in nanoelectronics circuits.

B. Emerging physical effects

In this section we describe several emerging physical phenomena that become to play an essential role in the operation of ultra-short devices, as well as the physical models which can be used in simulation for taking these phenomena into account.

Quantum confinement: The aggressive scaling-down of metal oxide semiconductor field-effect transistors (MOSFETs) in the deep submicrometer domain requires ultrathin oxides and high channel doping levels for minimizing the drastic increase of short channel effects. The direct consequence is a strong increase of the electric field at Si/SiO_2 interface, which creates a sufficiently steep potential well for inducing the quantization of carrier energy (Fig. 6). Carriers are then confined in a vertical direction in a quantum well (formed by the Silicon conduction band bending at the interface and the oxide/Silicon conduction band-offset) having feature size close to the electron wavelength. This gives rise to a splitting of the energy levels into subbands (two-dimensional (2-D) density of states) [57]-[58], such that the lowest of the allowed energy levels for electrons (resp. for holes) in the well does not coincide with the bottom of the conduction band (resp. the top of the valence band). In addition, the total density of states in a 2-D system is less than that in a three-dimensional (3-D) (or classical) system, especially for low energies. Carriers occupying the lowest energy levels behave like quantized carriers while those lying at higher energies, which are not as tightly confined in the potential well, can behave like classical (3-D) particles with three degrees of freedom (Fig. 6). As the surface electric field increases, the system becomes more quantized as more and more carriers become confined in the potential well. The quantum mechanical confinement considerably modifies the carrier distribution in the channel: the maximum of the inversion charge is shifted away from the interface into the Silicon film (as shown in Fig. 6). Because of the smaller density

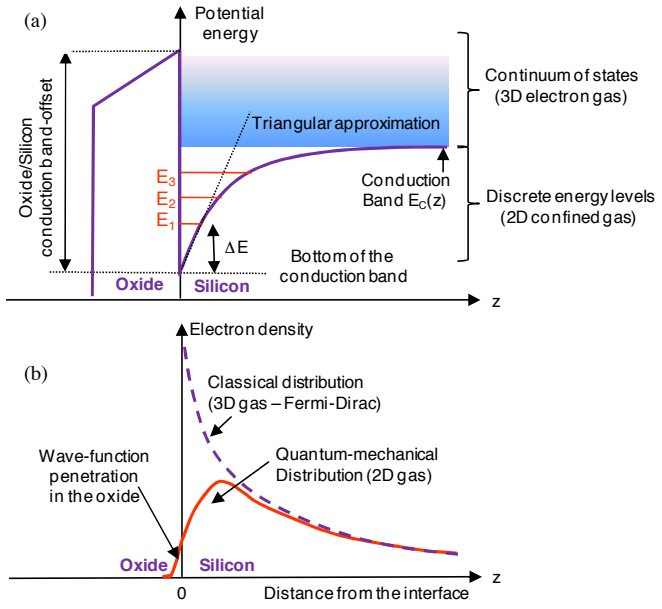

Fig. 6. (a) Schematic illustration of the conduction band bending of a MOS structure in inversion regime showing the different energy levels resulting from the quantization effects of the 2-D electron gas confined in the surface potential well. (b) Corresponding electron distributions in the direction perpendicular to the interface for the classical and quantum-mechanical cases.

of states in the 2-D system, the total population of carriers will be smaller for the same Fermi level than in the corresponding 3-D (or classical) case. This phenomenon affect the net sheet charge of carriers in the inversion layer, thus requiring a larger gate voltage in order to populate a 2-D inversion layer to have the same number of carriers as the corresponding 3-D system. This leads to an increase of the threshold voltage of a MOSFET, which is an important issue, especially as the power supply voltages drop to lower levels. The gate capacitance and carrier mobility are also modified by quantum effects. These considerations indicate that the wave nature of electrons and holes can no longer be neglected in ultra-short devices and have to be considered in simulation studies. Quantum confinement becomes also important for the device response to single event. A detailed study of quantum confinement effects on the immunity to single-event of SOI Single-Gate and Multiple-Gate devices will be presented in section II (part I).

Various methods have been suggested to model these quantum confinement effects. Among the approaches that are compatible with classical device simulators based on the drift-diffusion or hydrodynamic approaches, the physically most accurate method is to include the Schrödinger equation into the self-consistent computation of the device characteristics [59]. However, solving the Schrödinger equation in itself is very much time-consuming. Various simpler methods have been suggested, such as the Van Dort model or the Hansch model. The van Dort model [60] expresses quantum effects by an apparent band edge shift that is a simple function of the electric field. The model is based on the expression for the lowest eigenenergies of a particle in a triangular potential well (Fig. 6). Although van Dort model reproduces well the characteristics obtained with the Schrödinger equation, it does not give the correct charge distribution in the device. The Hansch [61] model proposes a quantum correction of the density of states as a function of depth below the Si/SiO_2 interface. The charge distribution is better reproduced, but the model strongly overestimates the impact of quantum confinement on the drain current characteristics.

An alternative to take into account quantum confinement is the Density-Gradient model [44]-[49], coupled with the Drift-Diffusion or the hydrodynamic transport equations. Density-Gradient model considers a modified equation of the electronic density including an additional term dependent on the gradient of the carrier density. Then, a potential-like quantity Λ is added in the classical electron density formula, as follows:

$$n = N_C \exp\left(\frac{E_{Fn} - E_C - \Lambda}{kT}\right) \tag{14}$$

where n is the electron density, T is the carrier temperature, k is the Boltzmann constant, N_C is the conduction band density of states, E_C is the conduction band energy, and E_{Fn} is the electron Fermi energy. The impact of the quantum confinement on the carrier density in the device can be taken into account by properly modeling the quantity Λ. For Density Gradient model, Λ is usually given in terms of a partial differential equation:

$$\Lambda = -\frac{\gamma\hbar}{6m}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \tag{15}$$

where $\hbar = h/2\pi$ is the reduced Planck constant, m is the electron density of states mass, and γ is a fit factor. Equations similar to (14) and (15) apply for the hole density. These new equations for electron and hole densities are then used in the self-consistent solving of Poisson equation and of the transport equation (Drift-Diffusion or hydrodynamic).

Ballistic and quasi-ballistic transport: Drift-diffusion and hydrodynamic models fail at describing ballistic transport. The highest value of drain–source current which can be obtained for a given MOSFET geometry corresponds to the pure ballistic current limit. As the channel length is increased, the current decreases from this maximum value due to scattering effects. The transport makes a transition from the ballistic to quasi-ballistic or drift- diffusive regime with the longer channel lengths. The carrier transport in the channel is considered to be ballistic when carriers travel from the source to the drain regions without encountering a scattering event. This may be possible if the feature size of the device becomes smaller than the carrier mean free path [19]. If the carrier transport is purely ballistic in the channel, modeling the device behavior reduces to the description of the carrier transmission over and through the source-to-drain potential barrier. Fig. 7 illustrates the source-to-drain potential energy profile in the channel of a nanotransistor (biased in its on-state) and the essential mechanisms governing the quantum transport of carriers. The amplitude and the width of the channel barrier are modulated by the gate and drain voltages. Carriers having energy higher than the maximum of the barrier, E_{max}, are transmitted from source to drain by thermionic emission, while carrier with lower energy can traverse the channel only by quantum mechanical tunneling through the source-to-drain barrier. Similar mechanisms can be also considered for electrons in the drain reservoir. Quantum reflections of carriers (i.e. wave-packets) also occur on the barrier not only at the extremities of the source and drain reservoirs but also in the channel, due to the potential energy drop induced by the source-to-drain voltage (Fig. 7). These reflections can impact both the tunneling and thermionic components of the pure ballistic response of the nanotransistor.

Numerous analytical and compact models of the ballistic and the quasi-ballistic transport have been proposed [62]-[65]. Some models take into account only thermionic emission [63], others additionally

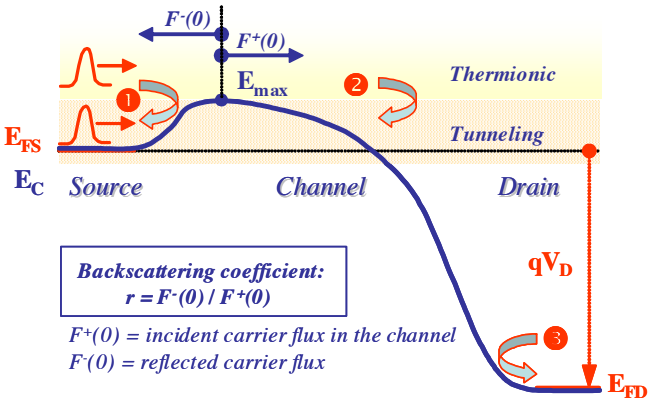

Fig. 7. Schematic representation of the source-to-drain potential energy profile in a nanotransistor (on-state) and illustration of the essential mechanisms governing the quantum transport of carriers. Quantum reflections of carriers (i.e. wave-packets) can occur on the barrier not only at the<< extremities of the source (1) and drain (3) reservoirs but also in the channel (2), due to the potential energy drop induced by the source-to-drain voltage. These reflections can impact both the tunneling and thermionic components of the pure ballistic response of the nanotransistor.

consider quantum mechanical tunneling [64]. This later phenomenon was shown to be a fundamental physical limit for MOSFET scaling below 6-8 nm gate length. Other models take into account quasi-ballistic transport, such as the general model based on the scattering theory which covers the full range from the ballistic to diffusive regimes [65]-[66]. Full 2-D and 3-D numerical codes that treat quantum transport, optionally including scattering effects, have been also developed, in the frame of NEGF formalism or Monte-Carlo/Wigner approaches [35], [50]-[55]. Although great effort has been made in this topic in the last decade, ballistic transport is not yet included in commercial simulation codes. How quasi-ballistic and ballistic transport will influence the future device immunity to irradiation is an open question which has to be addressed in future specific simulation studies.

C. 2-D versus 3-D simulation

The phenomena related to an ionizing particle striking a microelectronic device are naturally 3-D mechanisms, due to both the tri-dimensional structure of the ion track and the 3-D structure of real devices. 3-D simulation is not only necessary for actual short/narrow devices, but also for new device architectures for which 3-D electrostatic or quantum confinement effects cannot be taken into account in a 2-D simulation. 3-D simulation is also necessary when considering non-normal incidence of the ion strike on the device.

The earliest works for device simulation consisted of one-dimensional drift-diffusion models [67]. These 1-D device models have evolved to 2-D device modeling approaches based on either drift-diffusion equations or advanced hydrodynamic and energy balance models. Many charge collection and SEU studies have been performed using these models. It has been shown that in a 2-D rectangular simulation either the correct generated charge density or the correct total charge can be simulated, not both [15]. Different modified 2-D codes have been proposed in order to correct the geometry effects (scaling schemes that adjust Auger recombination rate [68], the use of quasi-3-D codes based on cylindrical symmetry and coordinate transformation [69]). A lot of studies have been performed using these 2D codes and valuable results and insights have been obtained; however, these codes can be only used for particular devices.

The first fully 3-D codes were developed in the 1980s [70], but optimized 3-D codes running on desktop workstations have been commercially available only recently [36]-[38], typically in the last decade (mainly due to the enormous progress of microprocessor performances). A comparison of 2-D and 3-D charge-collection simulations has shown that while the transient responses were qualitatively similar, quantitative differences existed in both the magnitude of the current response and the time scale over which collection was observed [71]. The comparison implies that 2-D simulations can provide basic insight while 3-D simulations become necessary when truly predictive results are to be obtained [15].

D. Ion track structure

The ion track structure to be used as input in simulation is presently a major issue for device simulation. The first representations included a simple cylindrical charge generation with a uniform charge distribution and a constant LET along the ion path. However, the real ion track structure is radial and varies as the particle passes through the matter. When the particle strikes a device, highly energetic primary electrons (called δ rays) are released. They generate further a very large density of electron-hole pairs in a very short time and a very small volume around the ion trajectory, referred as the ion track. These carriers are collected by both drift and diffusion mechanisms, and are also recombined by different mechanisms of direct recombination (radiative, Auger) in the very dense core track, which strongly reduces the peak carrier concentration. All these mechanisms modify the track distribution in time and space. As the particle travel through the matter, it loses energy and then the δ-rays become less energetic and the electron-hole pairs are generated closer to the ion path. Then, the incident particle generates characteristic cone-shaped charge plasma in the device [15].

The real ion track structure has been calculated using Monte-Carlo methods [72]-[74]. These simulations highlighted important differences between the track structure of low-energy and high-energy particles, even if the LET is the same (for details see [15], [75]). High-energy particles are representative for ions existing in the real space environment, but they are not available in typical laboratory SEU measurements [13]. Then the investigation of the effects of high-energy particles by simulation represents an interesting opportunity, which may be difficult to achieve experimentally.

Analytical models for ion track structure have been also proposed in the literature and implemented in simulation codes. One of the most interesting models is the "non-uniform power law" track model, based on the Katz theory [76] and developed by Stapor [77]. In this model, the ion track has a radial distribution of excess carriers expressed by a power law distribution and allows the charge density to vary along the track (i.e. the LET is not constant along the track) [78]-[79]. Other analytical models propose constant radius non-uniform track or Gaussian distribution non-uniform track.

In commercial simulation codes, the effect of a particle strike is taken into account as an external generation source of carriers. The electron-hole pairs generation induced by the particle strike is included in the continuity equations via an additional generation rate. This radiation-induced generation rate can be connected to the parameters of irradiation, such as the particle LET (defined as energy lost by unit of length - dE/dl). The particle LET can be converted into an equivalent number of electron-hole pairs by unit of length using the mean energy necessary to create an electron-hole pair (E_{ehp}) [80]:

$$\frac{dN_{ehp}}{dl} = \frac{1}{E_{ehp}} \frac{dE}{dl} \tag{16}$$

where N_{ehp} is the number of electron-hole pairs created by the particle strike. By associating two functions describing the spatial and temporal distributions of the created electron-hole pairs, the number of electron-hole pairs is included in the continuity equations via the following radiation-induced generation rate:

$$G(w,l,t) = \frac{dN_{ehp}}{dl}(l) \cdot R(w) \cdot T(t) \tag{17}$$

where R(w) and T(t) are the functions of spatial and temporal distributions of the radiation induced pairs, respectively. Equation (17) assumes the following hypothesis: the spatial distribution function R(w) depends only on the distance traversed by the particle in the material and the generation of pairs along the ion path follows the same temporal distribution function in any point. Since function G must fill the condition:

$$\int_{w=0}^{\infty} \int_{\theta=0}^{2\pi} \int_{t=-\infty}^{\infty} G w dw d\theta dt = \frac{N_{ehp}}{dl} \tag{18}$$

functions R(w) and T(t) are submitted to the following normalization conditions:

$$2\pi \int_{w=0}^{\infty} R(w) w dw = 1 \tag{19}$$

$$\int_{t=-\infty}^{\infty} T(t) dt = 1 \tag{20}$$

The ion track models available in commercial simulation codes usually propose a Gaussian function for the temporal distribution function T(t):

$$T(t) = \frac{e^{-(\frac{t}{t_C})^2}}{t_C\sqrt{\pi}} \tag{21}$$

where t_C is the characteristic time of the Gaussian function which allows one to adjust the pulse duration. The spatial distribution function is usually modeled by an exponential function or by a Gaussian function:

$$R(w) = \frac{e^{-(\frac{w}{r_C})^2}}{\pi r_C^2} \tag{22}$$

where r_C is the characteristic radius of the Gaussian function used to adjust the ion track width.

Previous works have demonstrated that the different charge generation distributions used for the radial ion track does affect the device transient response, but the variation is limited to 5% for ion strikes on bulk p-n diodes [15], [78]. Considering a LET which is not constant with depth along the path has a more significant impact on the transient response in bulk devices. The key parameters of the single event transient (peak current, time to peak and collected charge) have up to 20% variation when LET is allowed to vary with depth compared to the case of a constant LET [78]. Nevertheless, the LET variation with depth has no influence on the transient response of actual SOI devices with thin Silicon film.

II. Illustrations at device level for advanced SOI technologies

A. SEE mechanisms in SOI technologies

SOS (Silicon-on-Sapphire) and SOI technologies have been initially proposed as a solution to the problem of bulk devices sensitivity to ionizing irradiations [81]. In bulk Silicon devices, more than 99.9% of the substrate volume is not used and becomes a source of parasitic effects, such as leakage currents, latch-up, etc. The SOI materials eliminate this inconvenient, since the SOI structure itself is based on the principle of separation between the active region (the Silicon film) and the inactive substrate by a more or less thick insulator layer (the buried oxide). Then, there is no parasitic PNPN structure leading to single-event latchup (SEL) in CMOS/SOI devices. In the 1970s and 1980s, SOS and SOI technologies were primarily (exclusively) used for space and military applications. But, besides their natural radiation hardness, it was observed that the parasitic capacities of SOI MOS devices are lower than those of bulk MOS devices, due to the existence of the buried oxide. This leads to enhanced speed performances for SOI circuits. Later, it was shown that the power dissipated in SOI technologies is strongly reduced compared to bulk Silicon, and that higher integration density is obtained with SOI. All these advantages make SOI technology to gradually become a very attractive candidate for VLSI integrated circuits fabrication. After more than three decades of materials research and device studies, SOI wafers have definitively entered into the mainstream of semiconductor electronics. SOI MOSFET shows enhanced short-channel effects immunity and offers new potentiality for extending Silicon devices into the nanometer region (sub-20 nm channel length). Concerning the sensitivity to radiation, the charge collection in SOI devices is limited to the Silicon film which is very thin compared to bulk Silicon devices. This makes SOI device naturally hardened to single-event effects. However, the unique configuration of SOI MOSFET's is responsible for novel mechanisms (such as floating-body) not occurring in the bulk Silicon technology. The floating-body is at the origin of several parasitic phenomena specific to SOI devices like drain current overshoots and undershoots [82]-[83] or bipolar amplification. This last phenomenon is essential for the sensitivity of SOI devices and circuits to single-event [84]-[87]. As it will be explained in the following, SOI devices are not inherently immune to the radiation environment due to bipolar amplification, although they have less sensitive volume than bulk Silicon devices.

There are two major types of SOI NMOS and PMOS transistor structures: fully depleted and partially depleted. The full or total depletion of the film depends on the Silicon film thickness and doping level. Fully depleted (FD) SOI devices are usually designed with very thin films that are totally depleted in standard operation mode. In partially depleted (PD) SOI MOSFETs with submicron length, the lateral bipolar transistor (source-body-drain) can be easily turned on. The basic mechanism of the bipolar amplification is the following: the heavy-ion strike on the device creates electron-hole pairs in the Silicon film. While minority carriers recombine quickly, the lifetime of majority carriers in the body region can be very long. Majority carriers that do not recombine can drift toward the source region and raise the body potential. Then, the source-to-body potential barrier is lowered, which triggers the lateral parasitic bipolar transistor inherent to the SOI transistor. The potential raise is maintained until majority carriers are recombined. The bipolar current amplifies the collected charge and decreases the SEU/SET immunity, especially at low LET [88]. This effect is further enhanced by impact ionization mechanism induced by the high electric field at the body-drain junction. The consequence is that the SOI immunity to radiation is degraded; although SOI devices have a smaller sensitive volume than bulk Silicon devices, this is counterbalanced by the enhanced bipolar amplification [84]-[88].

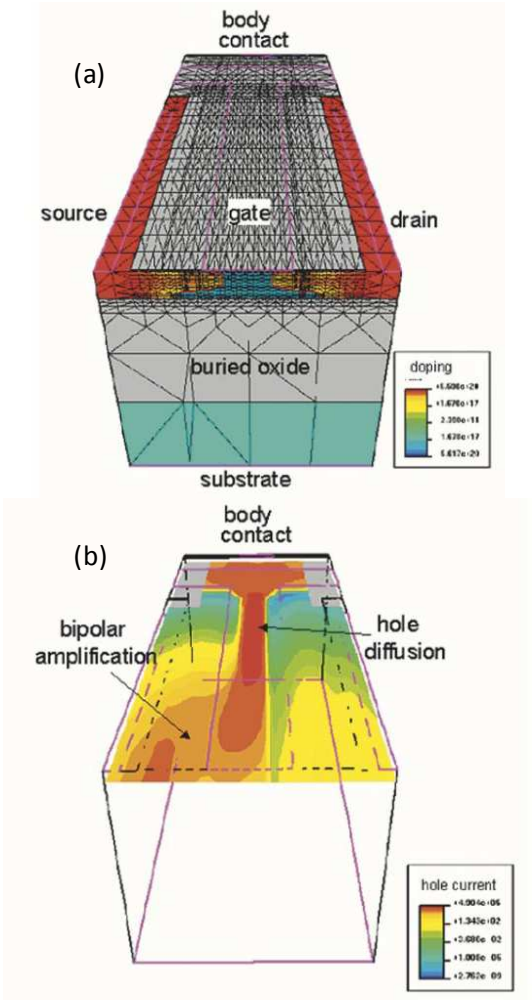

Fig. 8. Three-dimensional mesh and doping concentration (a) and hole current distribution (b) during a transient irradiation of a 0.25 μm SOI NMOSFET with external body contact. After Ferlet-Cavrois *et al*. [86]. © 2002 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

To reduce these bipolar effects, the most common technique involves the use of body ties (which connect the floating body region to a fixed potential). The excess holes created by the ion strike no longer accumulate in the floating body region because they are evacuated through the body contact. This reduces considerably the parasitic bipolar transistor effects. However, body ties do not completely eliminate the bipolar effect; a voltage drop exists along the body tie due to its finite resistance, and the reduction of bipolar effect is less effective. The ability of body ties to suppress the bipolar effect strongly depends on the location of the body tie in relation to the ion strike [89]. The farther the ion strike is from the body tie, the larger the effect of the parasitic bipolar transistor [84], [87], [90]-[91].

Numerical simulation at device level has been widely used in literature for the study of bipolar transistor and its effects on the sensitivity of SOI devices to ionizing radiation. For example, the occurrence of bipolar amplification in spite of body ties has been simulated in [86] and illustrated in Fig. 8 for a 0.25 μm gate length SOI PD n-channel MOSFET. Fig. 8(a) shows the mesh and the doping concentration in the simulated device and Fig. 8(b) illustrates the hole current distribution in the device after the body irradiation. The parasitic bipolar transistor appears far from the body contact, near the source to body junction, due to the accumulation of

holes after irradiation. Holes are also generated by impact ionization near the high-electric field region near the drain junction. Fig. 8(b) highlights the holes diffusion mechanism toward the body contact. The duration of this mechanism is relatively high (about several nanoseconds), which explains the possible bipolar conduction [86], in spite of the existence of the body tie.

Bipolar amplification can also occur in fully depleted transistor circuits. Previous experimental and theoretical studies have shown that, generally, fully depleted SOI-based devices exhibit reduced floating body effects and then lower bipolar amplification of the collected charge than partially-depleted SOI devices [84], [92]-[93]. The bipolar transistor mechanism in fully depleted devices has been explained in [43] using Monte Carlo simulations of 0.25 μm fully depleted SOI circuits: after irradiation of a n-channel MOSFET biased in its off state, excess holes are accumulated in the channel (mainly near the gate oxide) and lower the potential barrier; then electrons diffuse from source to drain to maintain the electrical neutrality. This mechanism is comparable to the bipolar transistor effect in partially depleted SOI devices [84]-[85]. Because bipolar amplification is less important for fully depleted than for partially depleted transistors, circuits based on fully depleted transistors are less sensitive to single-event upset than partially depleted circuits [93].

The effect of the parasitic bipolar transistor in SOI devices is quantified using the bipolar gain, β. The bipolar gain corresponds to the amplification of the deposited charge and is given by the ratio between the total collected charge, Q_{coll}, at the drain electrode and the deposited charge, Q_{dep}:

$$\beta = \frac{Q_{coll}}{Q_{dep}} \tag{23}$$

The total collected charge at the drain electrode is obtained using the equation:

$$Q_{coll} = \int_0^t I_D dt \tag{24}$$

The deposited charge in a SOI device is calculated as a function of the particle LET using the following equation [94]:

$$Qdep[\,fC\,] = 10.3 \times LET[\,MeV/(mg/cm^2)\,] \times t_{Si}[\,\mu m\,] \tag{25}$$

where t_{Si} is the Silicon film thickness and 10.3 is a multiplication factor for Silicon (calculated using the Silicon density and the energy needed for creating an electron-hole pair in Silicon – 3.6 eV – [94]). In this equation a normal incident ion strike is considered and the LET is supposed constant along the ion path in the active Silicon film.

When a heavy ion strikes an SOI MOSFET in the off-state, a drain current transient is observed at the drain terminal. This type of transient has been thoroughly investigated in literature in both partially depleted and fully depleted SOI transistors. It is well-known that these transients have two components: (i) a prompt component due to the discharge of excess electrons immediately after the ion strike and (ii) a slow-decay current due to floating body effects (charge amplification due to and parasitic bipolar effect). Recently, by separating these current components in the time domain, Kobayashi *et al.* have shown in [95] that the drain current transient has not two but three components: the two components reminded above and an additional slow-decay component. The investigation of the difference between the electron current flowing through the drain terminal and that through the source terminal has revealed the existence of this new component, as shown in Fig. 9(a). This third component is a second discharge current of a portion of the deposited electrons that is stored in the high-injection condition body to maintain quasi-neutrality. It was shown in [95] that this discharge current drastically expands the transient pulse width [Fig. 9(b)]. Since the pulse width is an important feature of single event transient (as discussed in part II),

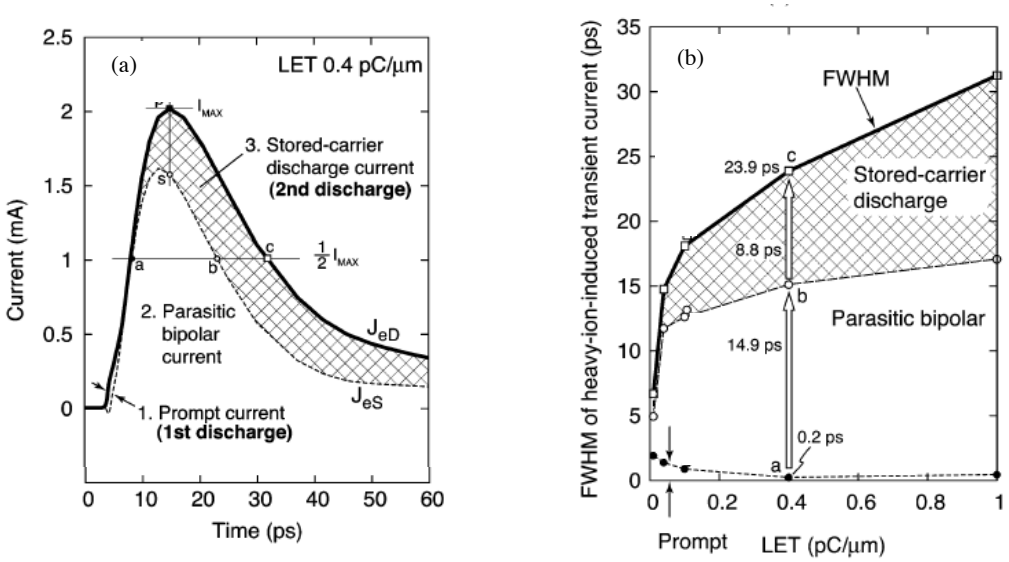

Fig. 9. (a) Time evolution of currents induced by a heavy-ion strike with LET = 0.4 pC/μm. J_{eD} is the electron current at the drain electrode and J_{eS} is the electron current at the source. (b) Impact of each current component on heavy-ion-induced transient currents. Pulse widths (FWHM) are plotted as a function of LET. After Kobayashi *et al*. [95]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

this third current component must be carefully taken into account in single event effects analysis. Finally, Kobayashi *et al*. analyses the effects of the device downscaling on this new transient component. Their investigation shows that the stored-carrier discharge current has the possibility to become a serious component for future miniaturized SOI MOSFET.

B. Simulation study of Fully-Depleted SOI technologies

In this section we present our recent simulation results concerning single-event transients in 50 nm ultra-thin (11 nm thick Silicon film) FD Single-Gate (SG) SOI MOSFET [96]. 3-D quantum numerical simulation has been used to highlight the influence of quantum confinement effects on carrier distribution and their consequences on the charge collection as compared to the "classical" (i.e. without quantum effects) case. The simulation results have also been compared to experimental data measured by heavy ion experiments performed at GANIL (Grand Accélérateur National d'Ions Lourds, Caen, France) on 50 nm FD SG SOI devices. A detailed description of the experimental set-up and measured data can be found in [96]. The tested devices are floating body (without body contacts) NMOS transistors fabricated with a fully depleted (FD) single-gate SOI technology [97]. The transistors have been processed with a mid-gap TiN gate, and the Silicon film is nearly intrinsic (P-type, 10^{15} cm^{-3}). The thicknesses of the Silicon film and of the buried oxide are 11 nm and 100 nm respectively and the equivalent gate oxide thickness is close to 1.8 nm.

The schematic description of the 3-D SOI architectures considered in the simulation is represented in Fig. 10(a). 3-D numerical simulations have been performed with the 3-D Synopsis tools (Dessis module)

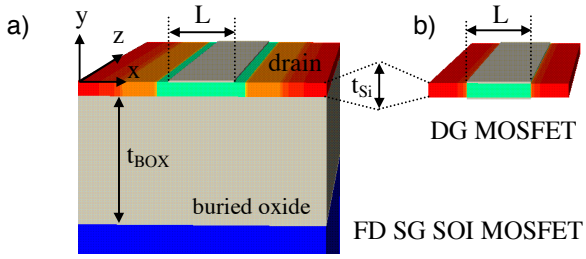

Fig. 10. Schematic description of the simulated 3-D FD Single-Gate SOI and Double-Gate devices. The doping levels of the colored regions are: green regions - 10^{15} cm^{-3}, orange regions - 5×10^{18} cm^{-3}, red regions - 10^{20} cm^{-3}. After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

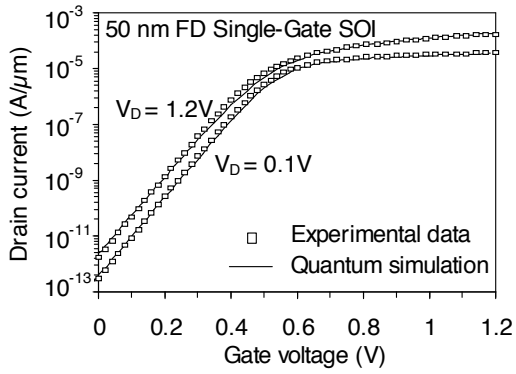

Fig. 11. Calibration of the simulated quantum-mechanical drain current on experimental data in 50 nm FD Single-Gate SOI devices. After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

[36] and with our homemade full quantum Fortran code BALMOS3D [98]. In 3-D Synopsis simulation, quantum confinement of carriers is taken into account using Density Gradient model, described in part I (section I.B). It has been shown [49] that the Density Gradient model can accurately account for quantum carrier confinement in Single-Gate SOI and Double-Gate devices with an appropriate calibration step of the fit factor γ [see Eq. (15)]. In [96] the exact solution of the Schrödinger–Poisson system of equations (as given by BALMOS3D) has been used for calibrating the Density Gradient model. The code BALMOS3D [98] used in this study is a homemade full quantum Fortran simulator, that solves self-consistently the 1-D Schrödinger equation and the 3-D Poisson equation on a 3-D-grid. The solution of this system of equations is coupled with the Drift-Diffusion transport equation in the channel.

The calibration step has been performed on 50 nm and 80 nm gate length devices having 11 nm thick Silicon film. For each particular device, the fit factor γ has been then finely tuned in order to obtain a perfect match between the characteristics calculated with BALMOS3D and that simulated with Synopsis tools. Additionally to the Density Gradient model, the physical models considered in the Synopsis code include the SRH and Auger recombination models and the Fermi-Dirac carrier statistics. Both the impact ionization and the carrier mobility depend on carrier energy calculated with the hydrodynamic model. The mobility model also includes the dependence on the lattice temperature and on the channel doping level. The physical parameters in simulation have been calibrated in order to fit the simulated quantum drain current on the experimental data. Fig. 11 shows the result of this calibration step performed on 50 nm FD SG SOI devices. The calibrated physical parameters have been further used in the simulation of drain current transients produced by an ion strike on the sensitive regions of the device. The drain current transients have been simulated in two cases: the classical case (i.e without quantum effects) and in the quantum case. The transistors were simulated biased in the off-state (most sensitive case).

The simulated irradiation track has a Gaussian shape with narrow radius of 14 nm and Gaussian time dependence, centered on 50 ps and with a characteristic width of 2 ps. We have chosen this small radius value in order to be comparable with the actual radii used in the experiment. We also considered an angle of incidence of the ion strike of 60°, as in the heavy ion experiment [96]. The deposited charge was

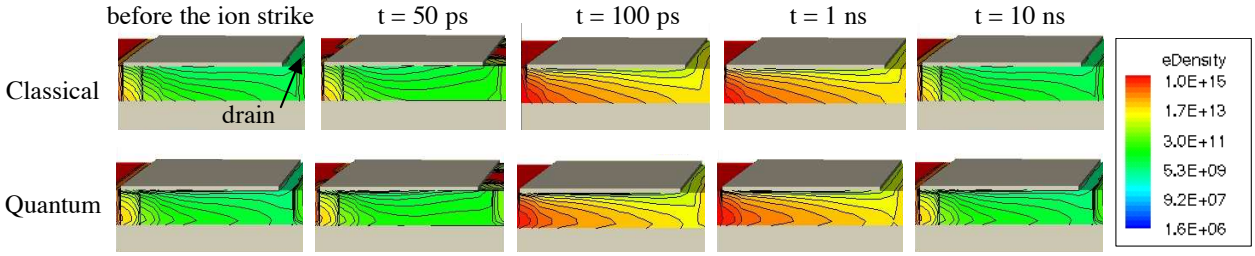

Fig. 12. 3-D electron density distribution (expressed in cm^{-3}) in the Silicon film in 50 nm FD Single-Gate devices (V_G = 0 V, V_D = 0.7 V) at different times before and after the ion strike. After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

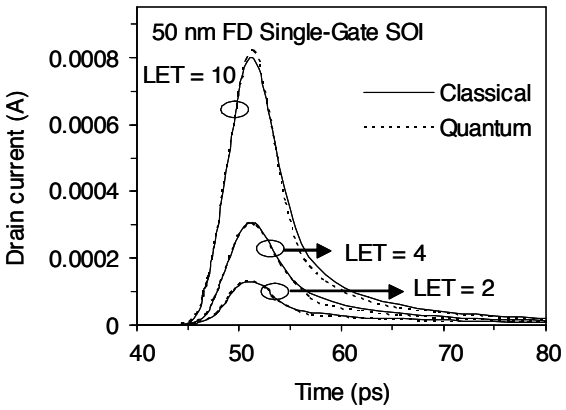

Fig. 13. Drain current transient at different LET values in 50 nm FD Single-Gate SOI. The LET values are expressed in MeV/(mg/cm^2). After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

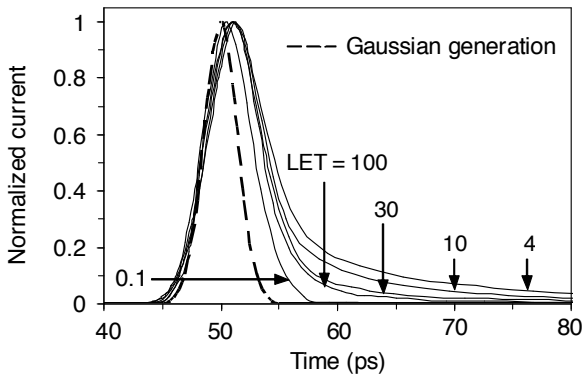

Fig. 14. Normalized drain current versus time in the quantum case at different LET values expressed in MeV/(mg/cm^2). After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

calculated considering the Gaussian distribution and the 3-D geometry of the Silicon film. The collected charge and the bipolar gain are obtained using equations (24) and (23), respectively.

3-D carrier density distributions simulated in classical and quantum simulations are compared in [96] (Fig. 12). The maximum of the inversion charge is located at the interface between the Silicon channel and the gate oxide in the classical case, whereas in the quantum case the charge density is very low at the interface and its maximum is moved inside the Silicon film at several nanometers depth [see also Fig. 6(b)]. The total inversion charge is lower in the quantum case than in the classical case, thus the threshold voltage increases and the drain current value in the off-state is lower in the quantum case than in the classical case. This is an important issue, since the value of the drain current in off-state was shown to affect the collected charge and the bipolar amplification of the device [99]. The drain current transients due to the ion strike in the classical and quantum cases are compared in Fig. 13 for different LET values. Quantum transients have current prompt component and transient tail similar to the classical case. Simulations presented in [96] show that the transients are even almost identical at very high LET values, where the charge generation is significant and masks the impact of the different carrier distributions in the channel between the quantum and classical cases. The quantum drain current transients have been normalized to their peak value and have been compared to the initial Gaussian time-dependent charge generation (Fig. 14). The quantum drain current transient at low injection regime LET = 0.1 MeV/(mg/cm^2) is almost synchronous with the charge generation, which illustrates a weak bipolar amplification. At high LET, the drain current peak is shifted and is clearly wider than the Gaussian generation, indicating a high bipolar amplification.

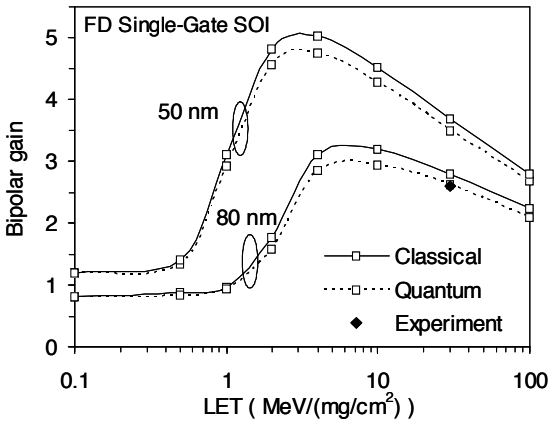

Fig. 15. Bipolar gain in FD Single-Gate SOI devices for two gate lengths: 50 nm and 80 nm. The experimental bipolar gain obtained at LET = 30 MeV/(mg/cm^2) on 80 nm FD SG SOI device is also reported. The angle of incidence in both experiment and simulation is 60°. After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

The collected charge and the bipolar gain (Fig. 15) are lower in the quantum case, mainly due to the lower off-state current. For 80 nm gate

length device and for an ion strike near the drain with a LET = 30 MeV/(mg/cm^2) the bipolar gain is 2.8 in the classical case and about 2.62 in the quantum case. This last result is in excellent agreement with the experimental results (bipolar gain of 2.6 in worst case [96]).

C. FD Single-Gate SOI versus Double-Gate configuration

In FD SG SOI MOSFETs the differences in the bipolar gain between classical and quantum cases are quite limited, due to the relatively thick Silicon channel (11 nm) and to the Single-Gate configuration. This difference is clearly larger when considering Double-Gate devices and thinner Silicon channel thicknesses. In this case the potential well becomes rectangular and induces stronger quantization effects than in devices with a Single-Gate configuration [100]-[101].

Double-Gate devices are presently considered as the most promising solution for continuing the MOSFET scaling towards nano-scale dimensions [102]-[103]. These devices need very thin Silicon films in order to reinforce the electrostatic control of the two gates over the channel and then to eliminate short-channel effects. In this way, Double-Gate devices could be designed with intrinsic channels, offering then an enhanced mobility, the elimination of doping fluctuations and a high probability of ballistic transport. In return, the use of ultra-thin channels implies the existence of huge quantum-mechanical confinement effects. In [96] the quantum behavior of ultra-thin Double-Gate devices submitted to heavy ion irradiation is investigated and compared to that of Single-Gate devices.

The Double-Gate structure simulated in [96] is schematically described in Fig. 10(b). The electron density profile [Fig. 16(a)] in a vertical cut-line in the middle of the channel along the y axis shows that the electron density is maximum at the two interfaces in the classical case. In the quantum case, the density profile shows two maxima situated within the Silicon film at several nanometers depth from the interface. Fig. 16 is typical for Double-Gate devices with thin Silicon film [104]. The drain current in the quantum case is splitted in two separate channels, but they are no more located at the interface as in the classical case. When the Silicon film is thinned down the effect of quantum confinement is enhanced. In the case of a very thin film [Fig. 16(b), t_{Si} = 5 nm], the two electron density maxima in the quantum case are superposed in the middle of the Silicon film. Then a unique conduction channel, located in the middle of the film, exists for the electron transport from source to drain. Similar to the case of Single-Gate devices, the total quantum inversion charge (and the drain current) is lower than the classical one for a given gate and drain bias. Fig. 17 shows the drain current as a function of the gate voltage for two Silicon film thicknesses. In the classical case, the subthreshold drain current is higher for the 11 nm thick film than for the 5 nm thick film. This is the result of the volume inversion, which is a key phenomenon in the operation of Double-Gate and multi-gate devices. In the subthreshold regime, carriers flow from source to

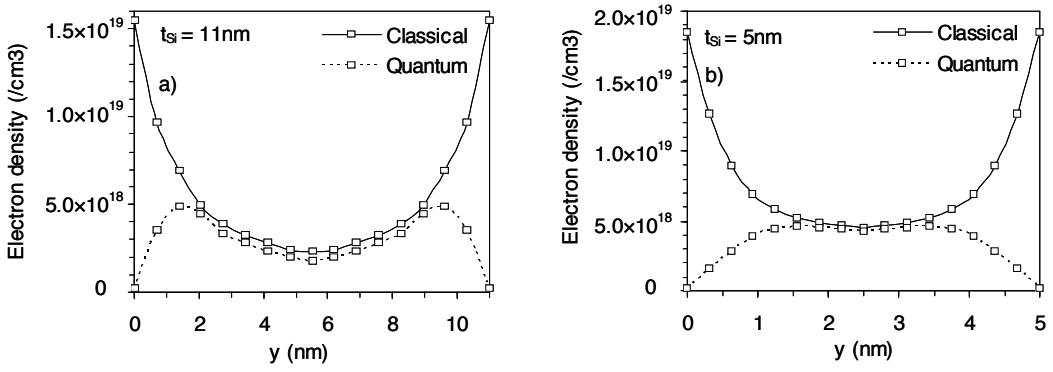

Fig. 16. Electron distribution in a vertical cut-line (parallel to y axis) in the middle of the channel for Double-Gate devices with 11 nm (a) and 5 nm (b) thick Silicon channel (on-state operation $V_D = V_G = 0.7$ V). After [96].

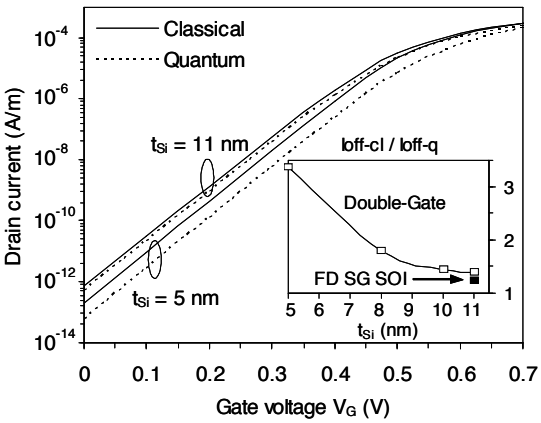

Fig. 17. Drain current characteristics as a function of the gate voltage in classical and quantum cases for Double-Gate devices with t_{Si} = 11 nm and t_{Si} = 5 nm. The ratio between the classical off-state current (Ioff-cl) and the quantum off-state current (Ioff-q) is also reported in the inset as a function of the film thickness. After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

drain over the entire film thickness and the drain current is directly proportional with t_{Si}. Fig. 17 also shows that the quantum drain current curves are shifted to higher gate bias with respect to the classical curves for both film thicknesses. Then the quantum off-state current is lower than the classical one. The ratio between the classical and quantum off-state currents (inset of Fig. 17), confirms that the quantum confinement is considerably enhanced when the film is thinned down. This ratio is about 1.3 for a film thickness of 11 nm and sensibly increases when reducing this thickness down to 5 nm. For this very thin film the quantum off-state current is more than three times lower than the classical one. Since the off-state current is a key parameter in the device response to single-event, this analysis demonstrates the necessity of taking into account quantum confinement in the simulation of very thin Double-Gate devices. Fig. 18 shows the variation with time (after an ion strike) of the electron density distribution in classical and quantum cases for t_{Si} = 11 nm and in the quantum case for t_{Si} = 5 nm. Here (and everywhere in the analysis of heavy ion irradiation) the device is considered in the off-state. In the quantum case carriers are more centered in the middle of the film and the volume inversion phenomenon is reinforced. In the same time the total inversion charge is lower than in the classical case.

The bipolar gain is found to be lower in Double-Gate than in Single-Gate configuration, mainly due to the better electrostatic control of the channel which reduces floating body effects [96]. The bipolar gain decreases in 5 nm thick Double-Gate compared to 11 nm thick Double-Gate, as a result of both a lower deposited charge and a reduced floating body effect. In [96] is also shown that the difference of the bipolar gains between classical and quantum case is significantly higher in Double-Gate than in Single-Gate devices (Fig. 19). Contrary to Single-Gate devices, the quantum bipolar gain in DG transistors exceeds the classical gain at medium and high LET. The maximum value of the gain in the quantum case is also shifted towards higher LET values, which is consistent with simulation results obtained in Multiple-Gate nanowires MOSFETs (presented in the next paragraph [100]). These differences come not

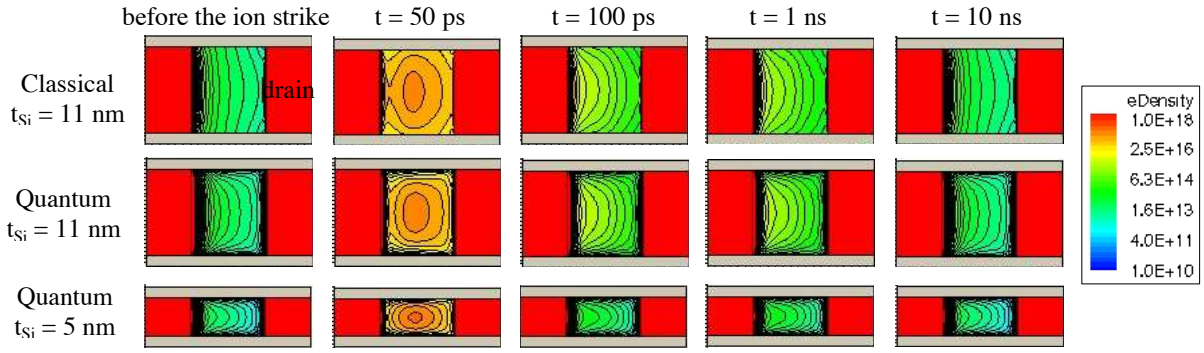

Fig. 18. Classical and quantum electron density (expressed in cm^{-3}) in a vertical cross-section along the source-drain axis (x-y plane) in the Silicon film of 50 nm Double-Gate devices with 11 nm and 5 nm thick channels. LET = 10 MeV/(mg/cm^2). After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

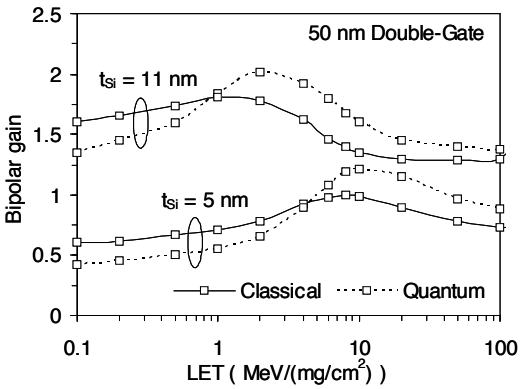

Fig. 19. Bipolar gain as a function of LET in 50 nm Double-Gate devices for different Silicon film thicknesses. After [96]. © 2006 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

only from a lower off-state current in the quantum simulation, but also from a different carrier distribution which modifies the recombination rate at the source end [100]. Note that the bipolar gain is quite low in DG devices, but the results are in good agreement with simulation data presented in [99] (classical case) and in [100] (both classical and quantum cases).

D. Simulation of multiple-gate nanowires MOSFET and trends for next technology nodes

Simulation in the 3-D device domain is the unique tool for exploring single-event effects in new device architectures which are not yet manufactured or for which compact models do not exist or are not sufficiently accurate. 3-D quantum simulation has been used in [100] for investigating the drain current transient produced by the ion strike in Multiple-gate nanowire MOSFETs with ultra-thin channels (≤ 10 nm). Multiple-gate nanowire MOSFETs are presently considered as one of the future possible solutions for replacing the bulk devices and continuing the MOSFET scaling in the nanometer scale [105]. A wide variety of architectures, including planar Double-Gate (DG) [102]-[103], [106]-[107], Vertical Double-Gate (VRG) [108]-[109], Triple-Gate (Tri-gate) [110], FinFET [111]-[114], Omega-Gate (Ω-Gate) [115], Pi-Gate (π-Gate) [116], Δ-channel SOI MOSFET [117], DELTA transistor [118], Gate-All-Around (GAA) [119]-[120], Rectangular or Cylindrical nanowires [121], has been proposed in the literature. These structures exhibit a superior control of short channel effects resulting from an exceptional electrostatic coupling between the conduction channel and the surrounding gate electrode. It has been shown that the electrostatic control is enhanced when increasing the "Equivalent

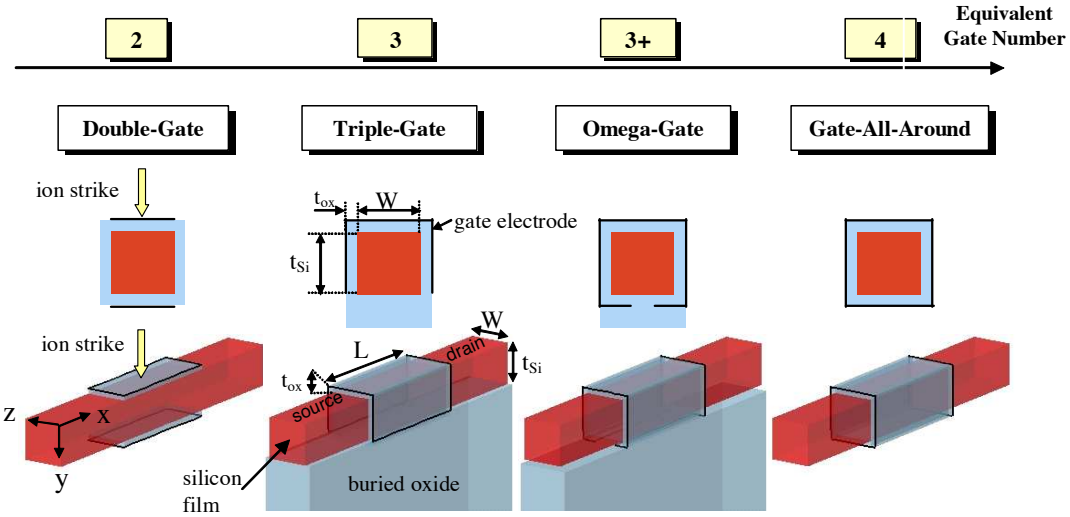

Fig. 20. Schematic description of the 3-D simulated DG, Triple-Gate, Omega-Gate and GAA structures and their main geometrical parameters. The devices are classified as a function of the "Equivalent Gate Number" (EGN). The schematic cross-sections in the (y-z) plane are also shown. For all the simulated structures, there is no gate overlap with the S/D regions and the S/D doping concentration is 10^{20}cm^{-3}. The position of the ion strike is also indicated by the arrow; the ion strikes vertically in the middle of the channel (between the source and drain region) and in a direction parallel to the y axis. The Silicon substrate was simulated for the Triple-Gate and the Omega-Gate structures. All structures have Silicon film with square section (t_{Si} = W). After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

Gate Number" (EGN) from 2 (for DG devices) to 4 (for GAA devices where the gate electrode is wrapped around the entire channel) [101].

As it will be explained later, quantum confinement effects are significant in Multiple-gate devices, due to both ultra-thin Silicon films and the existence of two confinement directions (for EGN > 3). Then it becomes mandatory to include quantum effects in the simulation of Multiple-Gate devices and circuits. The transient response of Multiple-Gate nanowire MOSFETs under heavy ion irradiation has been addressed in literature [122]-[124], but all the previous studies considered the "classical" approach. In [100] we investigated the impact of the quantum confinement on drain current transient and the bipolar amplification in Multiple-gate nanowire MOSFETs.

Four different Multiple-Gate configurations have been considered: Double-Gate, Triple-Gate, Omega-Gate and Gate-All-Around. The devices are calibrated to fill the ITRS'2006 [1] Low Power (LP) technology requirements for the technology nodes corresponding to the years 2007, 2009 and 2011. These devices are expected to be designed with 32 nm, 25 nm and 20 nm physical gate lengths, respectively. The description of the 3-D architectures considered in the simulation and the definition of their geometrical parameters are presented in Fig. 20. The Silicon film (considered with a square cross-section) and the gate oxide have the following dimensions: (a) t_{Si} = W = 10 nm and t_{ox} = 1.2 nm for the 32 nm node, (b) t_{Si} = W = 8 nm and t_{ox} = 1 nm for the 25 nm node and (c) t_{Si} = W = 5 nm and t_{ox} = 0.9 nm for the 20 nm node. All devices have intrinsic channel and mid-gap gate, and the thickness of the buried oxide is 100 nm. The supply voltage is 0.8 V for the 32 nm and 25 nm nodes and 0.7 V for the 20 nm node.

Similar to the study of FD SG SOI devices presented in the previous paragraph, a calibration step of the Density Gradient model on BALMOS3D has been performed in [100] for obtaining the fit factor γ. Fig. 21 schematically represents the quantum confinement directions in three different generic configurations: Single-Gate, Double-Gate and GAA devices. The impact of quantum effects on the electron density extracted along a cut-line parallel to the confinement directions is also illustrated. As

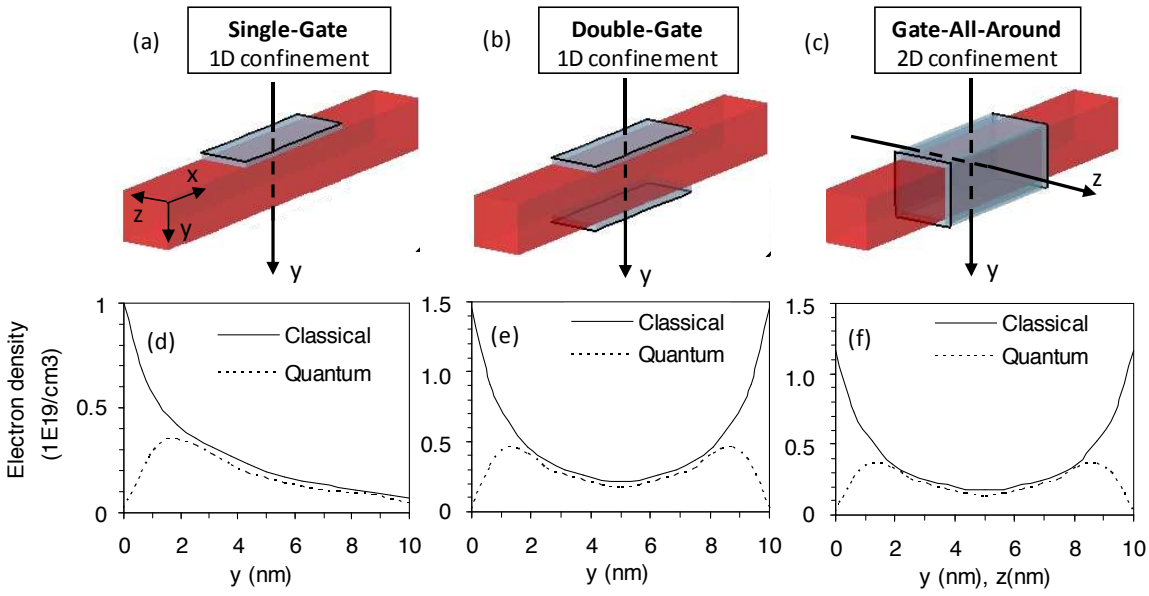

Fig. 21. Schematically representation of the quantum mechanical confinement directions in Single-Gate (a), Double-Gate (b) and Gate-All-Around (c) configurations. The profile of the carrier density in a cut-line along the film thickness is also reported for both classical and quantum cases: (d) Single-Gate, (e) Double-Gate and (f) Gate-All-Around. All devices are biased in the on-state. $V_D = V_G$ = 0.8 V, L = 32 nm. After [100].

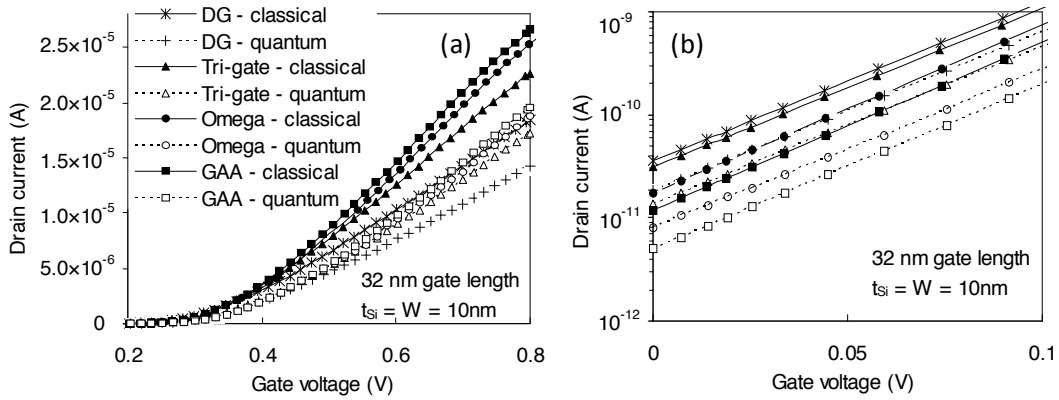

Fig. 22. Drain current $I_D(V_G)$ characteristics in classical and quantum mechanical cases for 32 nm DG, Tri-gate, Ω-Gate and GAA architectures (V_D = 0.8 V): (a) the above threshold regime; (b) zoom on the subthreshold characteristics. After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

shown in the previous paragraph, in Single-Gate devices carriers are confined in a narrow triangular potential well, formed at the Si/SiO_2 interface. The quantum carrier density in y direction is then modified as compared to the classical one: the classical electron density is maximal at the Si/SiO_2 interface, since the quantum density profile has a maximum shifted inside the Silicon film at several nanometers depth. In the case of a Double-Gate configuration, the potential well is rectangular and its size is now equal to the Silicon film thickness, which becomes a key parameter in the analysis of quantum effects. The electron density profile in quantum case presents two maxima situated within the Silicon film. In the Gate-All-Around structure carrier are confined in a double rectangular potential well (along the y and the z directions), which enhances considerably the quantum mechanical confinement. The carrier motion is no more free in the z direction (as is the case of the Single-Gate and the Double-Gate devices), but their energy in the z direction is quantized as that in the y direction. Both the gate electrode width (W) and the Silicon film thickness control here the quantum effects. The quantum electron density in the z direction is no more maximal at the interface but has two maxima located into the Silicon film as for the carrier density in the y direction (Fig. 21). Then the total inversion charge is lower than in DG configuration.

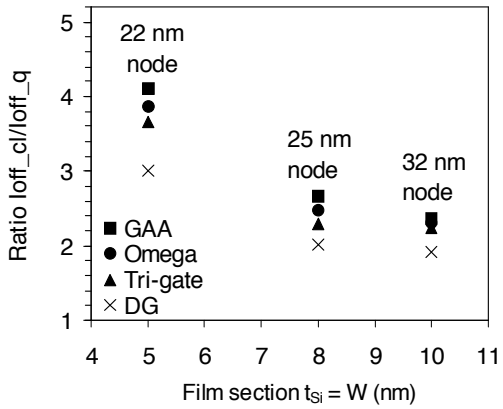

Fig. 23. Ratio of the off-state currents in classical (Ioff_cl) and quantum (Ioff_q) approaches. After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

$I_D(V_G)$ curves for the different 32 nm Multiple-Gate MOSFET architectures have been simulated in [100] in the classical and quantum cases [Figs. 22(a) and 22(b)]. The results shown that increasing the "Equivalent Gate Number" reduces the off-state current and improves the subthreshold swing S (S = 70 mV/dec for DG, S = 68.5 mV/dec for Triple-Gate, S = 65 mV/dec for Omega-FET and S = 61.5 mV/dec for GAA). This is due to the better electrostatic control of the gate over the channel that reduces the short channel effects. At the same time, the on-state current increases with EGN (Fig. 22), due to the multiple-channel conduction and to a better electrostatic control. As expected, the quantum current is lower than the classical one, because the total inversion charge is reduced in the quantum case.

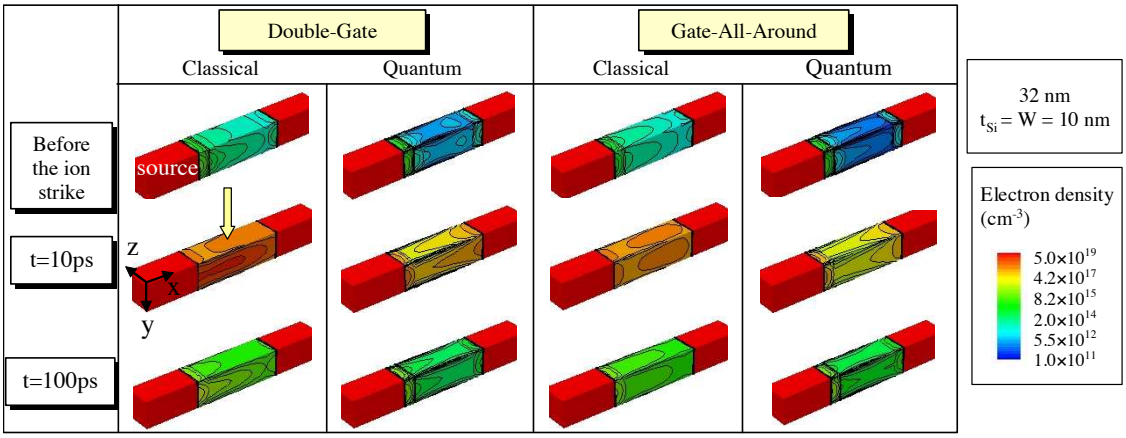

Fig. 24. 3-D electron density distribution (expressed in cm^{-3}) in the Silicon film of 32 nm DG and GAA in classical and quantum cases at different times before and after the ion strike. The ion track generation has a Gaussian time dependence centered at 10 ps and a strike LET of 1 MeV/(mg/cm^2). The devices are biased in the off-state at V_G = 0 V and V_D = 0.8 V. The gate oxide and the gate electrode are not shown. After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

The ratio between the classical and quantum off-state currents (Fig. 23) increases with EGN for a given technology node. This effect can be explained considering the dimensionality of the quantum confinement: in DG, carriers are confined in one direction (y direction), since in Triple- Gate, Ω-Gate and GAA carriers are confined in two directions (y and z), which strongly enhances the energy quantization with respect to DG.

The time evolution of the 3-D electron density in the Silicon film when an ion strikes vertically the middle of the channel of 32 nm DG and GAA devices has been also investigated in [100] (Fig. 24). The irradiation track has been simulated in a vertical incidence with a Gaussian shape (radius = 14 nm) and with a Gaussian time dependence, centered on 10 ps (characteristic width = 2 ps). Fig. 24 shows that in the quantum case the maximal value of the electron density is no longer located at the interface (as is the case in the classical approach) but into the Silicon film. This is also confirmed by the electron density distribution in a vertical cross-section (y-z plane) in the middle of the channel (Fig. 25): for all devices

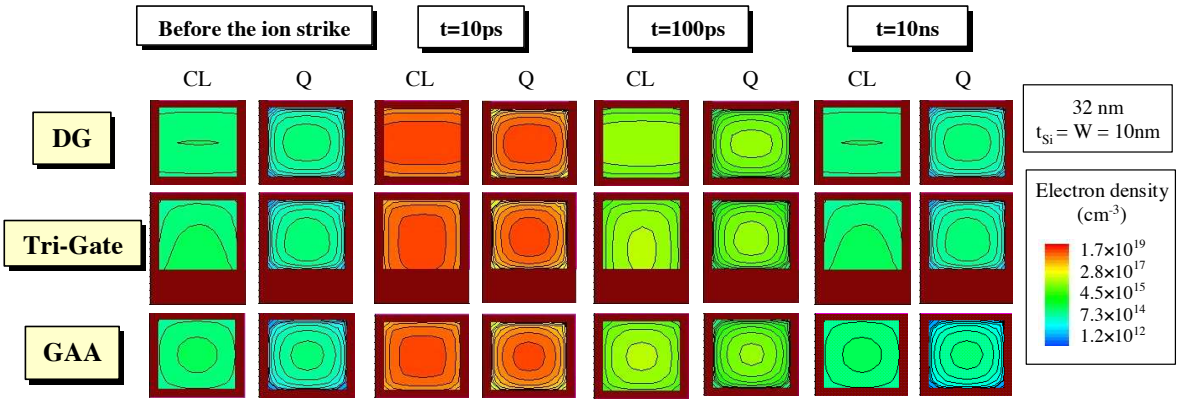

Fig. 25. Classical and quantum electron density (expressed in cm^{-3}) in a vertical cross-section (y-z plane) in the middle of the channel of 32 nm DG, Tri-Gate and GAA at different times before and after the ion strike. The brown regions represent the gate oxide (in DG and GAA devices) and the gate and buried oxide in Tri-Gate devices. After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

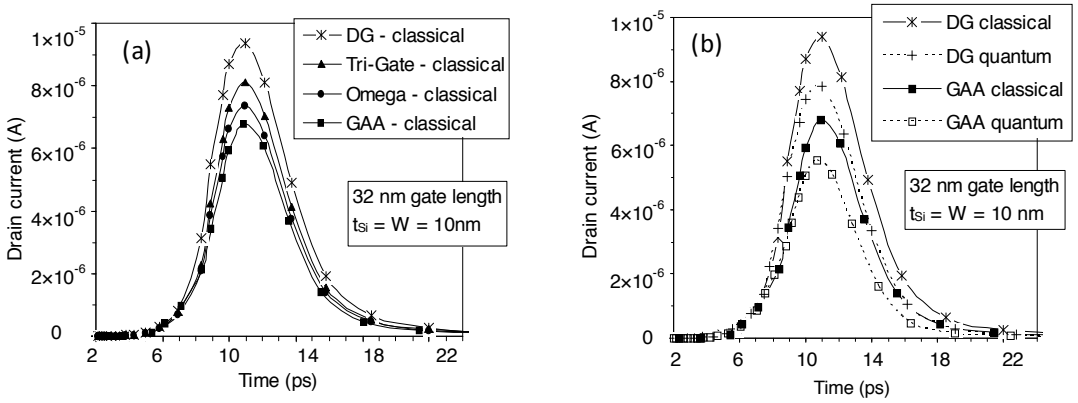

Fig. 26. Drain current transients induced by an ion strike vertically (y direction) in the middle of the Silicon film. LET = 1 MeV/(mg/cm^2). (a) Classical simulation in DG, Tri-Gate, Omega-Gate and GAA; (b) comparison between classical and quantum simulation in DG and GAA MOSFETs. All devices are off-state biased (V_G = 0 V, V_D = 0.8 V). After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

the quantum electron charge is centered in the middle of the film and the electron density has lower values than in the classical case. In off-state bias condition, the carrier conduction in all devices is mainly dominated by the volume inversion phenomenon: carriers flow from source to drain over the entire Silicon film thickness. Then the off-state current is directly proportional to the film thickness. In the quantum case the volume inversion phenomenon is reinforced because the quantum carrier density becomes more centered in the middle of the film (Fig. 25). This later effect is enhanced when EGN increases from 2 (DG) to 4 (GAA).

An illustration of the drain current transients simulated in [100] is presented in Fig. 26. Peak values of the drain current transient are reduced when EGN increases. The drain current transient tail is shorter when going from DG to GAA because the channel potential is better controlled by the gate when EGN increases and the floating body effects are reduced. The bipolar amplification (Fig. 27) decreases when increasing EGN due to less floating body effects. However, at high LET (> 2 MeV/(mg/cm^2)), the classical bipolar gain becomes the same for all configurations. This can be explained by the huge deposited charge by the ion which masks the influence of other phenomena such as the electrostatic control by the gate. The quantum bipolar gain is lower than the classical one, excepted at very high LET. Two phenomena, with opposite effects on the bipolar gain, are to be considered. On one hand, the lower off-state current in the quantum case leads to a lower quantum bipolar amplification. On the other hand, in the quantum case, the electron density is lower leading to slower recombination process (reflected in a longer transient tail) and then to a higher collected charge. Depending on the injection regime one phenomenon or the other prevails. At low injection regime, the generated charge is small and carriers recombine rapidly. Then the bipolar gain follows the off-state current behavior, both being lower for a

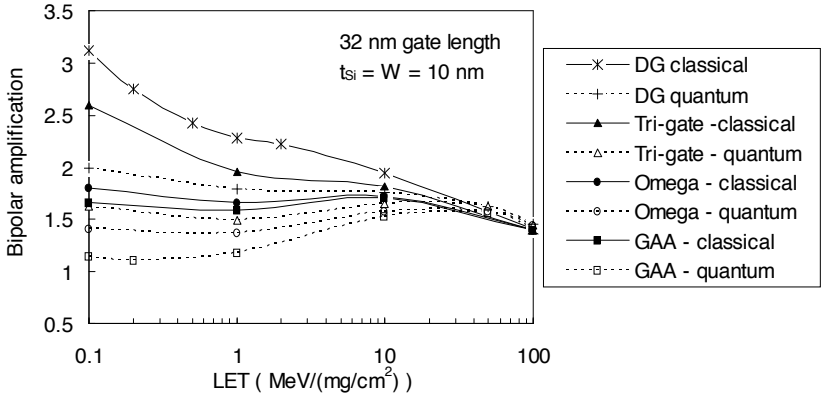

Fig. 27. Simulated classical and quantum bipolar gain as a function of LET in 32 nm gate length Multiple-Gate MOSFET corresponding to the ITRS LP technology node for the year 2007. After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

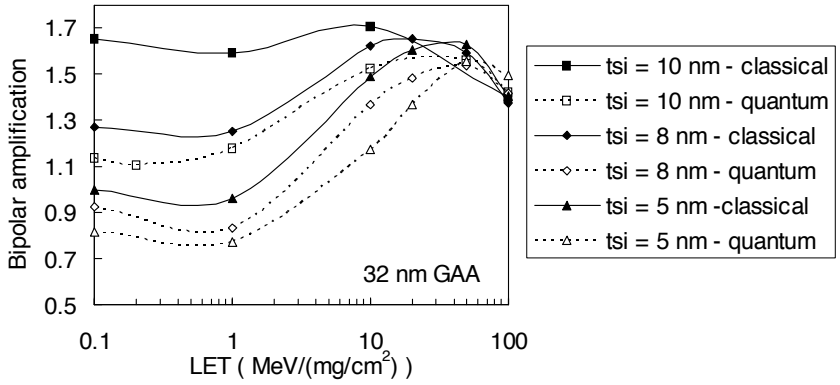

Fig. 28. Bipolar gain variation when reducing the Silicon film thickness in 32 nm GAA MOSFET (the gate width is W = 10 nm). After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

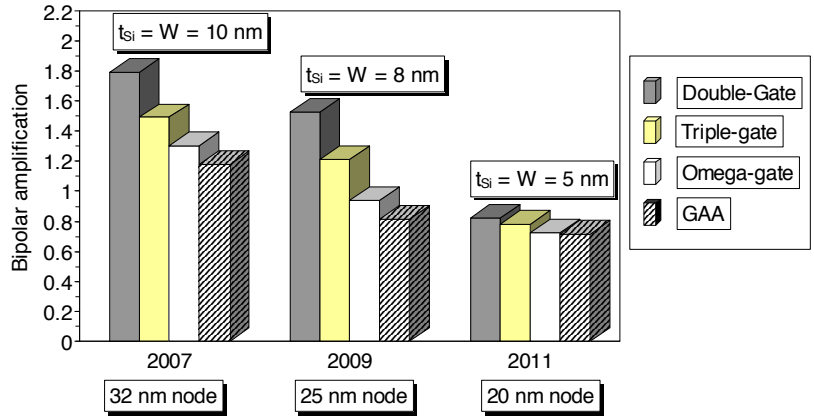

Fig. 29. Bipolar gain in multiple-gate nanowire MOSFETs as a function of the ITRS LP technology node in the quantum case. The ion LET is 1 MeV/(mg/cm^2). After [100]. © 2007 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

quantum approach than for a classical one. In very high injection conditions, the electron charge in the film is not sufficient to recombine the huge generated charge and then, the recombination process is sensibly slower. This has been verified by simulation in [100]: the recombination rate in the Silicon film is higher in the classical case than in the quantum case at the highest LET values. As a consequence, the quantum collected charge and the quantum bipolar amplification are higher than in the classical ones.

The simulations in [100] also shown that the effects of the carrier quantum confinement become more significant when the Silicon film is thinned. This is due to the energy subband splitting that is directly proportional with the reverse of the square of the potential well dimension (equal to the film thickness). The ratio between the classical and quantum off-state currents (Fig. 23) as a function of the Silicon film thickness confirms that the quantum confinement is strongly enhanced when the film thickness is reduced. The collected charge and the bipolar gain (Fig. 28) are lower for thinner channel (in both quantum and classical cases) because the off-state current decreases with the film thickness and floating-body are reduced.

Finally, the quantum bipolar gain for multiple-gate devices scaled down to 20 nm gate length and 5 nm × 5 nm Silicon film cross-section was also predicted in [100]. As shown in Fig. 29, the difference between the four architectures is reduced for the 2011 node compared with that for years 2007 and 2009, due to the very thin square wire cross-section. When decreasing the cross-section, the influence of the gate configuration is attenuated and the values of the bipolar gain for the different structures are almost the same. This behavior can be explained by the fact that, around 5 nm and below, the combination of gate electrostatic control and quantum mechanical confinement leads to similar carrier density distributions in the Silicon film for all gate configurations [101]. At this ultimate scale of integration, it should be expected that the sensitivity of all multiple-gate nanowire architectures (EGN ≥ 2) to heavy ion irradiation sensibly become equivalent.

PART II. CIRCUIT LEVEL MODELING

In this second part, we describe the different circuit-level modeling approaches of soft errors in integrated circuits. Due to the evolution of microelectronics, driven by the famous Moore's law, and to the sensitivity of recent technologies in terms of single-event effects, not only memory ICs but also high performance logic ICs must be henceforth considered to be potentially affected by SEE. This part of the short-course survey the circuit-level modeling approaches (circuit-level simulation, mixed-mode, 3-D simulation of full circuit) of single-event effects in integrated circuits. The SEE mechanisms in advanced SRAM and in logic circuits will be reminded. Digital Single-Event Transient (DSETs) production and propagation in sequential and combinational logic, as well as the soft error rate trends with scaling will be particularly addressed. Finally, recent bibliographical examples of simulation in SRAMs (bulk and Double-Gate) and logic circuits (flip-flops, inverter chains) are presented and discussed to illustrate these topics at circuit-level.

I. CIRCUIT MODELING APPROACHES

A. Circuit level

Circuit-level SEE simulation can be performed using standard simulation codes widespread in the IC industry for circuit design and optimization, such as the popular Berkeley SPICE, Silvaco SmartSPICE, Synopsys HPSICE, Orcad PSPICE, Mentor Graphics ELDO simulators, etc. Circuit simulators such as SPICE solve systems of equations that describe the behavior of electrical circuits (e.g. Kirchoff's laws …). Basic components of these simulation codes are compact models that describe the static/dynamic electrical behavior of the different elementary devices (transistors, diodes, resistors, etc.) constituting the circuit. Compact or circuit models are generally based on analytical formulae that approximate measured terminal characteristics. Advanced compact models provide high accuracy with minimum computational complexity. For simulating single-event effects at circuit level, the single-event induced transient is usually modeled as a current source connected at the struck node of the circuit [Fig. 30(a)]. This approach is adequate for many purposes, but presents some limitations. Firstly, it requires that satisfactory compact models already exist. But the use of compact models always introduces a certain numerical error (directly linked to the model accuracy), and models that are adequate for digital circuit simulation may be inadequate for other applications. Secondly, the accuracy of the transient current used as the input stimulus may considerably affect the circuit simulation precision. A typical example is the use of the current transient resulting from the device-level simulation of an unloaded device. In [125] the response of a memory cell to single-event is simulated at the circuit-level with Spice. The stimulus used at circuit level to reproduce the effect of the ionizing particle is a current pulse obtained by simulating at device level (2-D simulation with PISCES) the transient response of an unloaded device. In this case the circuit simulation inherits the inaccuracy of the improperly loaded device simulation [15].

B. Mixed-Mode technique

The limitations of compact models can be overcome by using physically-based device simulation to predict the response to ionizing radiation of the struck device. This approach is referred to as "mixed-mode" or "mixed-level" simulation, since the struck device is described by simulation in the device domain and the other devices by compact models. The two simulation domains are tied together by the boundary conditions at contacts, and the solution to both sets of equations is rolled into a single matrix solution [126]-[127]. Fig. 30(b) shows the construction of an SRAM cell in the frame of mixed-mode simulation. Only the struck transistor is modeled in the 3-D device domain. The current transient resulting from the ion strike on the struck device is directly computed by device domain simulation (there is no need for using an input stimulus which reproduces this current transient like in circuit-level simulation).

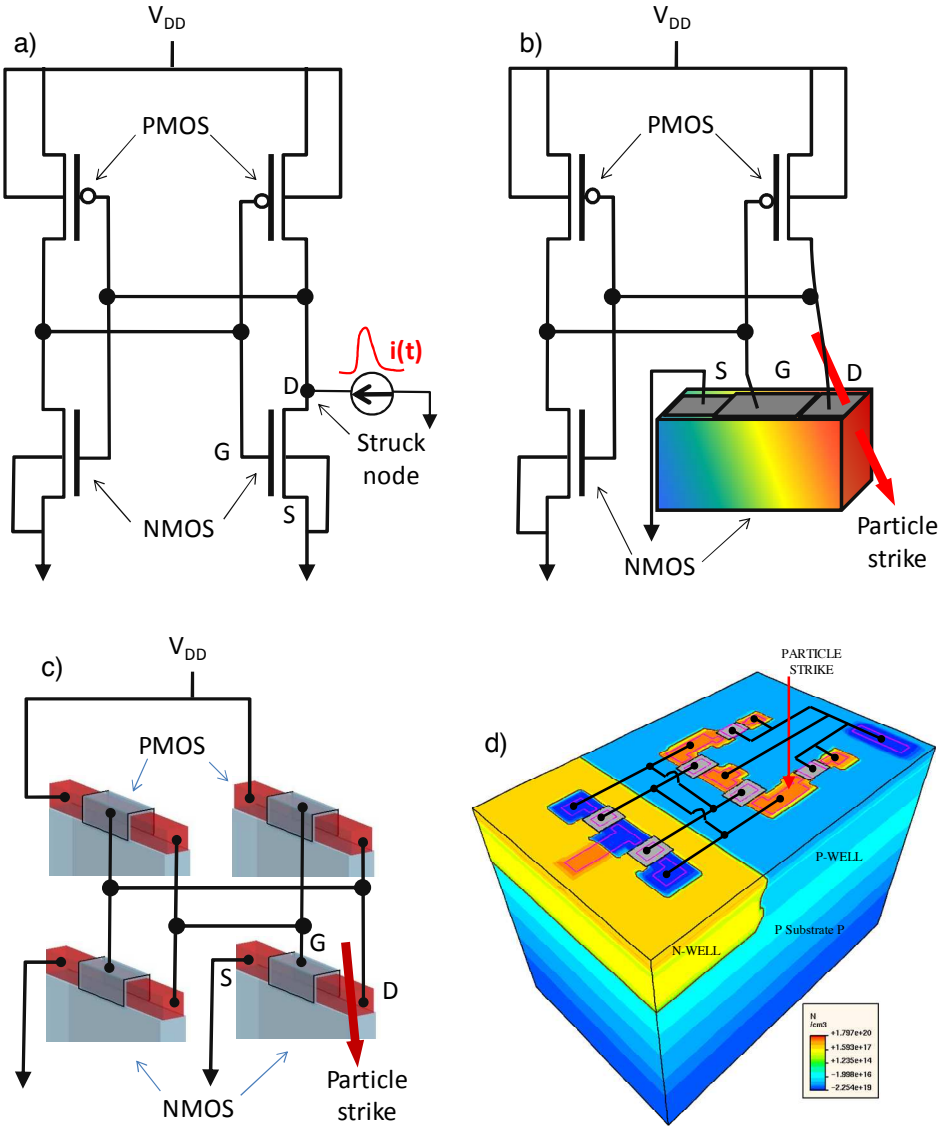

Fig. 30. Illustration of the simulation methods that can be used to investigate single-event effects at circuit level (here illustrated for a SRAM cell): (a) SPICE simulation; (b) mixed-mode simulation; (c) numerical simulation with several discontinuous domains connected using a mixed-mode approach; d) full 3-D numerical simulation with one continuous domain. The snapshot of the full 3-D 6T SRAM cell (d) is courtesy from P. Roche (STMicroelectronics) [80].

Mixed-mode capability is implemented in all major commercial device simulators [36]-[38] and is generally used for the study of circuits with a reduced number of devices (like SRAM cells). Mixed-mode simulation provides several worthwhile advantages. No compact model needs to be specified for a numerical physically-based device. The approximation errors introduced by compact models or by input stimulus can be avoided. One can also access the internal device quantities (such as potential, electric field, carrier densities) within a physically-based device-level simulation at any point during the circuit simulation. In addition, mixed-mode technique can typically be used to simulate ionizing radiation impact in new devices (such as ultra-scaled multiple-gate and Silicon nanowire devices) and/or for taking into account emerging physical phenomena (e.g. quantum confinement or quasi-ballistic transport) for which compact models do not exist or are not yet satisfactory. In this case, all transistors contained in an SRAM cell can be simulated in the 3-D device domain. For example, the circuit shown in Fig. 30(c) is used to

study the SEU sensitivity in SRAM cells based on GAA MOSFET with very thin Silicon film envisaged in the long term ITRS nodes [1].

The main inconvenient of the mixed-level simulation approach is the increased CPU time compared with a full circuit-level (SPICE) approach. In addition, mixed-mode simulation becomes not tractable for complex circuits. But, in the case of SRAM cells for example, the 3-D mixed-mode simulations need significantly reduced computing times compared with the numerical simulation of the full cell in the 3-D device domain. Finally, it is important to note that 3-D mixed-level simulation is accurate for SRAMs only in the case where there are no coupling effects between the devices [15]. Since the spacing between devices will decrease with pushing the integration level, it is expected that coupling effects will become more important, and simulating the cell in the device domain may become mandatory [128]-[130].

C. Full numerical simulation in the 3-D device domain

The most accurate solution for studying the SEU in SRAM is to numerically model the entire cell in the 3-D device domain. This was possible only recently (typically in the past decade), due to the enhancement of computer performances (CPU clock speed, memory resources) which reduced the computational time. Pioneering works of Roche *et al*. [128]-[129] and Dodd *et al*. [130] have demonstrated the capability of commercial codes to build and numerically simulate single-event-effects on complete 3-D SRAM cell. An example is shown in Fig. 30(d), with a full 3D 6T SRAM cell [80]. Although the simulation time needed for simulation of the entire cell in the 3-D device domain was substantially reduced, it is still considerable compared with the time needed to simulate the same circuit with Spice and mixed-level approaches. The recent emergence of PC-based parallel machines (clusters) with hundreds of processors and important memory resource is certainly one very promising way to develop in the future such full 3-D simulations on large scale circuits or, more reasonably, portions of circuits.

II. SEU MECHANISMS IN ADVANCED MEMORIES

A particle that strikes a sensitive region of an SRAM cell deposits a dense track of electron-hole pairs. If the collected charge at a particular sensitive circuit node exceeds the minimum charge that is needed to flip the value stored in the cell, a soft error occurs in the SRAM. An error due to a hit of a single particle is called a single event upset (SEU). Fig. 31 schematically shows a typical SRAM cell; when the word line (WL) is low the cell is holding its stored data using the back-to-back inverter configuration. If the particle strike causes a transient in one of the nodes, the disturbance can propagate forward through the CMOS inverter and induces a transient in the second node. The second node, in its turn, leads the first node towards a wrong value and consequently the two nodes will flip. Then, the memory cell will reverse its state and will store a false value [131]; there is no mechanism to restore its state other than explicitly rewriting the state via the bitlines. The SEU is a reversible phenomenon (the cell state could be recovered by a normal writing operation) which does not lead to the destruction of the cell. SEU can also occur when the particle strikes the bitline [131]-[132]. During the read operation, a bitline is discharged by a small current from a memory cell. The bit of information is read as a one a “0” or “1” based on the voltage differential developed on the bitline during the access period of the memory cell. This voltage differential is disturbed if a particle strikes close to a diode of an access transistor of any cell on this bitline. The smallest charge that results in a soft error is called the critical charge (Q_{crit}) of the SRAM cell. The rate at which soft errors occur is called Soft Error Rate (SER) and is typically expressed in terms of *Failures In Time (FIT)* (the number of failures per 10^9 hours of operation). Numerous approaches have been proposed for estimating the SER by simulation and dedicated simulation codes have been developed. The description of these SER codes is outside the scope of this short-course (for a detailed review we invite the reader to consult reference [133]). We simply remind here an

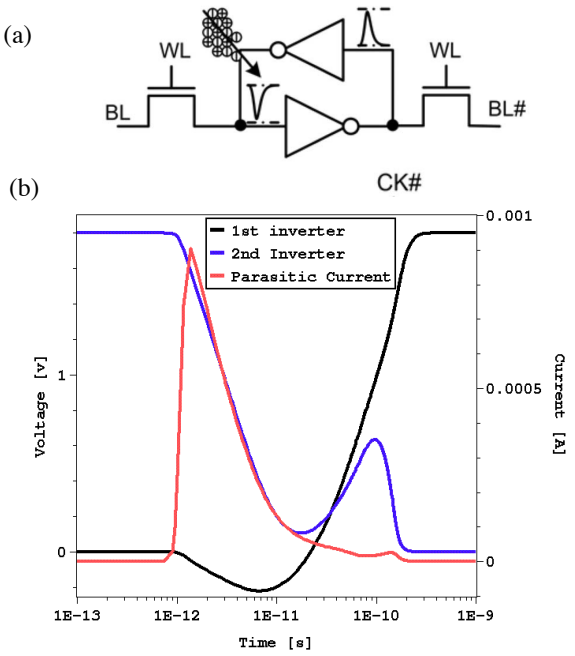

Fig. 31. (a) Schematic circuit for an SRAM cell and (b) illustration of the transient current induced by a particle strike. (a) is adapted after Karnik *et al*. [131]. © 2004 Institute of Electrical and Electronics Engineers Inc., reproduced with permission. (b) is courtesy from P. Roche (STMicroelectronics).

elementary analytical model for empirically estimating SER in CMOS SRAM circuits. This model developed by Hazucha and Svensson [134] was used to evaluate the effect of device scaling on the SER of memory circuits. In this model the SER is estimated by the following equation:

$$SER = K \times A \times F \times exp\left(-\frac{Q_{crit}}{Q_S}\right) \qquad (26)$$

where K is a scaling factor, F is the neutron or alpha flux in particles ($cm^{-2} \times s^{-1}$), A is the area of the circuit sensitive to particles strikes in cm^2, Q_{crit} is the critical charge in fC and Q_S is the charge collection efficiency of the device, in fC. The main advantage of Eq. (26) is that one can immediately identify the key parameters for SER in SRAM cells. In addition, this model can be used for the SER estimation in logic circuits (as it will be discussed in the paragraph IV.C), which makes possible a first-order comparison of SER in SRAM and sequential/combinational logic.

Two key parameters for SER are the critical charge (Q_{crit}) of the SRAM cell and the charge collection efficiency (Q_S) of the circuit. Q_S and Q_{crit} are determined by the process technology [134], whereas Q_{crit} also depends on characteristics of the circuit, particularly the supply voltage and the effective capacitance of the drain nodes. Q_{crit} and Q_S are essentially independent, but both decrease with decreasing feature size. Eq. (26) highlights that changes in the ratio $-Q_{crit}/Q_S$ will have a very large impact on the resulting SER. The SER is also proportional to the area of the sensitive region of the device, and therefore it decreases proportional to the square of the device size.

Circuit level simulation, mixed-mode approach or 3-D device domain simulation of the full cell have been largely used in the literature to study single-event effects in SRAM circuits designed in different CMOS technologies (see reviews in [133] and [135]). In the next sections we will remind some of these simulation studies.

A. Bulk and SOI SRAMs: SEU scaling trends

As noted in the precedent paragraph, sensitive area of an SRAM cell is a key parameter for the estimation of the error rate. The sensitive area cannot be predicted using standard single-point (i.e., one ion strike location) 3-D mixed-level simulations, even if these simulations are known to predict upset thresholds in very good agreement with measured thresholds [136]. Generally, simplified cross-section curves are estimated from theoretical and simulation results by making assumptions about the sensitive area [137]. Recently, Dodd *et al*. computed for the first time upset cross section of SRAM using 3-D device simulator running on a large parallel computer [130]. Fig. 32 shows the 3-D simulated SRAM cell which contained about 100 000 grid points with maximum grid spacing of 0.2 μm [130]. 3-D simulations were performed for ion strikes incident every 0.5 μm throughout the SRAM unit cell. These simulations allowed the authors to build a map of the SEU-sensitive area of the SRAM cell for a given ion and energy. By repeating these simulations for several ion/energy combinations, the evolution of the sensitive

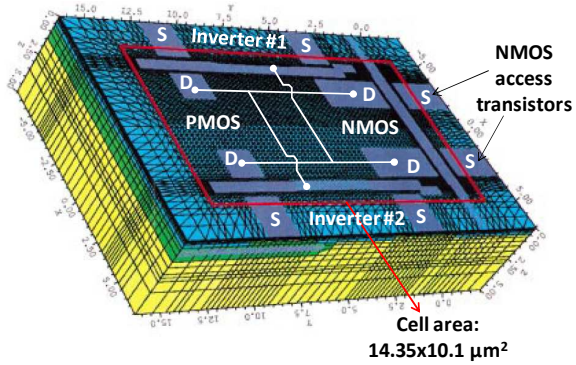

Fig. 32. Construction of the SRAM unit cell simulated in the 3-D device domain (D = drain and S = source). The red box indicates the boundaries of the unit cell. For this SRAM design, the NMOS pull-down transistors and the NMOS access transistors share common drains, and all source regions (PMOS and NMOS) are shared with the nearest neighboring cells. An additional 2 μm of Silicon was simulated around the unit cell to minimize nonphysical reflection of carriers at the boundaries. Adapted after Dodd *et al*. [130]. © 2001 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

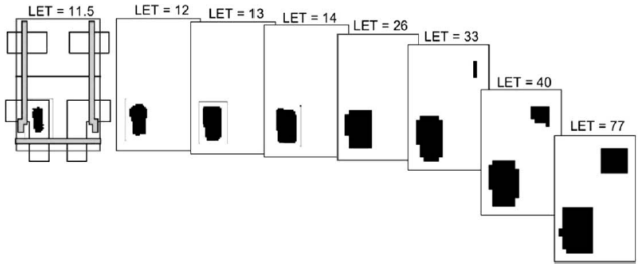

Fig. 33. Evolution of the soft-error sensitive area (black regions) of a 256K SRAM unit cell as a function of increasing ion LET. Adapted after Dodd *et al*. [130]. © 2001 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

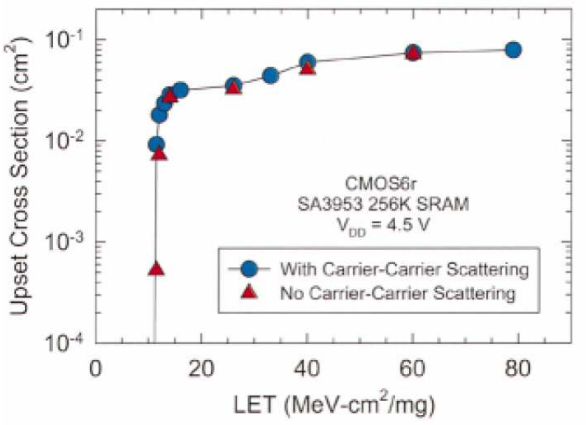

Fig. 34. Simulated upset cross section in a CMOS6r bulk 256K SRAM without feedback resistors. In this figure, the SEU-sensitive area per unit cell has been multiplied by 256K bits to arrive at the total IC cross section. Adapted after Dodd *et al*. [130]. © 2001 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

area as a function of ion LET was obtained, as illustrated in Fig. 33. This figure shows that for a LET value of 11.5 MeV/(mg/cm^2) (just above the upset threshold), the SEU-sensitive area is the center portion of the NMOS drain, which is expected to be the most sensitive strike location [136]. As the LET increases, the NMOS drain sensitive area increases and becomes even larger than the drain region itself at very high LET values. For a LET value of 33 MeV/(mg/cm^2) the PMOS drain becomes also sensitive to soft error. Finally, combining the information in the individual upset maps, Dodd *et al*. created a full upset cross section curve for the 256 K SRAM, as shown by the blue circles in Fig. 34 [130]. This curve was based on nearly 7000 individual soft error simulations, and took about three months on a parallel computer composed of 30 nodes. More details about the computational time and 3-D code used in these simulations are given in [130].

3-D mixed-level simulations were also used by Dodd in [15] to investigate the variation of the SEU threshold LET as a function of technology scaling for bulk and SOI technologies. The results are plotted in Fig. 35. The 3-D simulations predict an exponential drop in SEU threshold LET with gate length. For 0.18 μm bulk Silicon technology, the drain strike LET upset threshold is lower than 2 MeV/(mg/cm^2), then bulk Silicon circuit would be sensitive to alpha particle. The SOI circuit will probably become

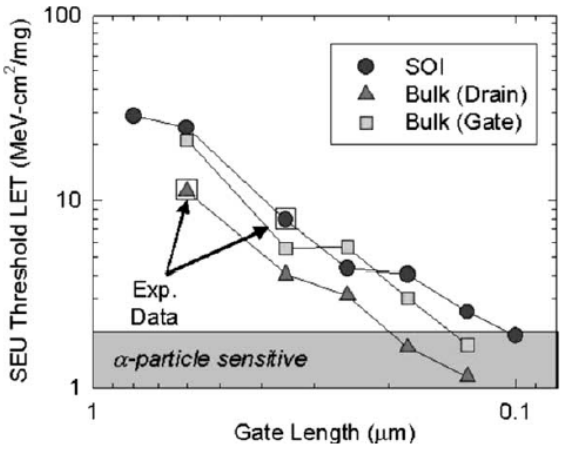

Fig. 35. Simulated LET threshold versus gate length trend for 6T SRAM cells in a bulk Silicon technology and a partially depleted SOI technology with body ties. The simulated devices are fully scaled (all parameters, gate length, supply voltage, doping level, etc., have been scaled). Predictions for the 0.6-μm and 0.35-μm technology nodes were validated against experimental data from Sandia fabricated technologies. After Dodd [15]. © 2005 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

sensitive to alpha particles for gate lengths around 0.1 μm. This is an important issue because α particles are one of the most abundant products resulting from the interaction of both proton and neutron with Silicon [15]. Alpha particles are also emitted from radioactive impurities in materials used in the chip package or from contamination of semiconductor processing materials. The prime source of alpha particle is from heavy elements and even the smallest trace contamination can cause serious problems [133]. High-energy alpha particles that strike the device deposit a dense track of charge as they pass through the Silicon substrate. The simulations performed in [15] suggest that future devices in bulk Silicon and SOI technologies will be very sensitive to SEU in both space and terrestrial environments. Finally, Fig. 35 shows that the gate strikes will become an important source of soft errors in bulk technologies (even if the drain is recognized as the most sensitive region in bulk devices): the threshold LET for gate strikes drops below the alpha-particle LET for the 0.13 μm node [15].

B. Simulation investigations for Double-Gate SRAM

Monte Carlo simulations were performed by Oldiges *et al*. in [138] to predict the SER of Double-Gate based SRAM cells. Soft error rates in conventional SOI circuit have been compared to SER for high mobility SOI and Double-Gate SOI designs. Strained Silicon-On-Insulator (SSOI) provides high mobility substrates which can enhance device performances (as explained in the introduction). Circuit simulations show that for the same cell design, a 0.13μm SSOI SRAM cell would have the same SER as conventional SOI cell. The simulations indicate that the use of high mobility devices has a negligible effect on the soft error rate and the reduction of the Silicon film thickness is expected to have a much larger impact.

Further, double gate structures with three different device architectures have been simulated [138] (Fig. 36): planar DG, FinFET and vertical Double-Gate (VRG) devices. The devices are fully depleted and two different Silicon thicknesses have been considered. The results of these simulations are

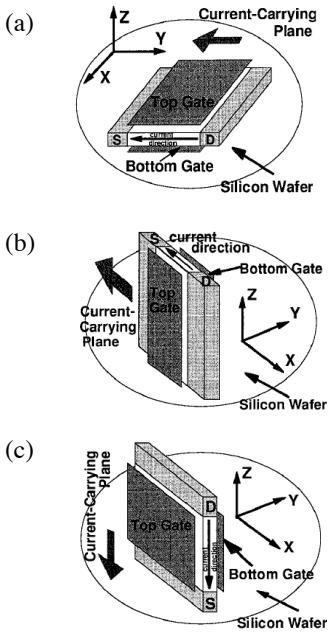

Fig. 36. Three different types of Double-Gate structures: (a) Planar DG, (b) FinFET, (c) Vertical DG. After Wong *et al*. [139]. © 1999 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

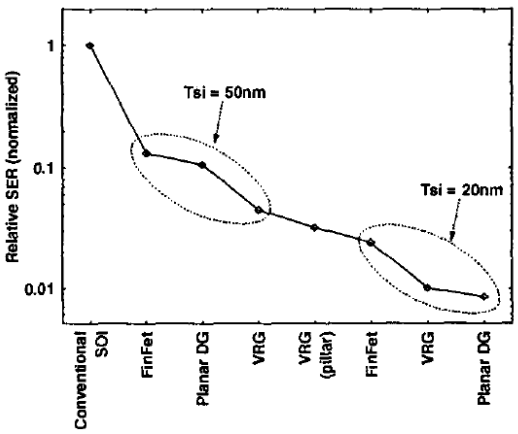

Fig. 37. Estimation of SER in various Double-Gate structures. The VRG pillar is a wrap-around-gate design. After Oldiges *et al*. [138]. © 2002 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

summarized in Fig. 37. The simulations show that the SER is improved by more than an order of magnitude in Double-Gate devices compared to FD Single-Gate SOI. The results also confirm that the thinner the Silicon film the higher the SER improvement [122].

The main conclusion of this study is that Double-Gate devices are expected to have an excellent soft error immunity since they are fully depleted (which reduces floating body-induced bipolar amplification) and have an extremely low sensitive volume due to thin Silicon bodies (which reduces the amount of generated charge). These results are consistent with simulations of Double-Gate devices in the 3-D device domain presented in part I (section II.B).

III. SEE MECHANISMS IN DIGITAL CIRCUITS

With the continuous decreasing of the CMOS feature size, it is well established that single event transients (SETs) become significant error mechanism and are of great concern for digital circuit designers. CMOS scaling is accompanied by higher operating frequencies, lower supply voltages, and lower noise margins which render the sensitivity of circuits SET increasingly higher [15], [140]–[149].

Digital single-event transients (DSETs) constitute a temporary voltage or current transient generated by the collection of charge deposited by an energetic particle. Even if this transient does not induce an SEU in the struck circuit, it can propagate through the subsequent circuits and may be stored as incorrect data when it reaches a latch or a memory element [15]. Unlike an SRAM cell (where an SEU occurs as a "persistent" error when a SET with sufficient charge impacts a critical node), in a combinational logic node an SET with sufficient charge may become manifested as a "persistent" error only if it propagates through the circuit and is latched into a static cell [148]. DSETs must fill a certain number of conditions in order to induce an error within a memory element [15], [150]:

(1) The ion strike must produce a transient able to propagate in the circuit.

(2) There must be an open logic path by which the DSET can propagate to reach a latch or a memory element.

(3) The DSET must have sufficient amplitude and duration to change the latch/memory state.

(4) In synchronous logic, the DSET must reach the latch during a clock pulse enabling the latch. Then the probability of capturing an SET increases with increasing clock frequency.

Digital circuits are constituted from sequential elements (e.g., latches, flip-flops, register cells) and combinational logic (e.g., NAND and NOR gates). The effects of single-event induced transients in these two types of circuits are succinctly described in the following.

A. Sequential logic

Typical sequential elements in the core logic are a latch [Fig. 38(a)], a domino cell [Fig. 38(b)] or a register file cell [Fig. 38(c)]. State changes can occur in core logic similarly to memory elements. In sequential logic (like in SRAM) the soft error rate has been found to be independent of the clock frequency of the circuit [151]. For example, the latch state can be flipped by the charge deposited by a particle strike on a circuit node regardless of the state of the clock signal.

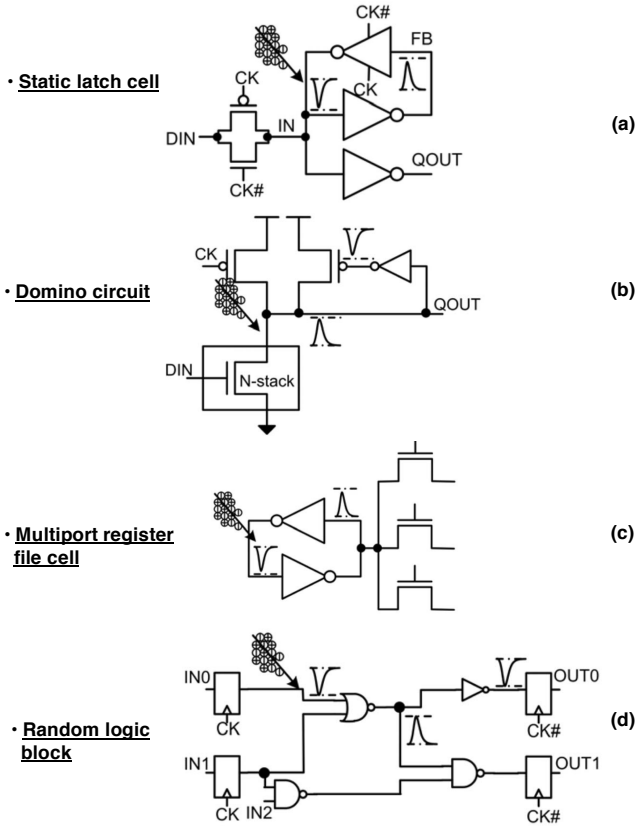

Fig. 38. Illustration of typical sequential logic (latch, domino, register) and combinational circuits (random logic block). Adapted after Karnik *et al*. [132]. © 2004 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

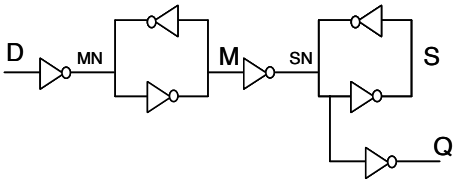

Fig. 39. Simplified schematic of the flip-flop circuit. The sensitive nodes are labeled as MN, M, SN and S. After Roche *et al*. [153]. © 2005 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

Flip-flop circuits (Fig. 39) are other typical sequential logic circuits. With technology scaling, flip-flops have become more susceptible to soft errors, mainly due to the decrease in supply voltage and in their node capacitances. The simplified schematics of Fig. 39 shows that flip-flops circuits are similar to SRAM cells, as both apply feedback loops of cross-coupled inverter-pairs. As noted in part II, the soft error sensitivity of this class of circuits is determined by the critical charge (Q_{crit}) and the collection efficiency (Q_S). In an SRAM cell Q_{crit} is mainly the same for the two storage nodes because the cell is symmetrical. In flip-flops, the inverters are sized differently and have different fan-outs, which makes the flip-flop circuit asymmetric compared to the SRAM cell. Then, the individual storage nodes in a flip-flop have a different critical charge than in a SRAM and their SER sensitivity can vary with several orders of magnitude [152].

B. Combinational logic

Any node in combinational circuit can be impacted by an SEU and cause a voltage transient which can propagate through the combinational stages [Fig. 38(d)] and causes an error if latched by a sequential element, such as a memory cell. In combinational logic a certain number of transients will not be latched and even latched, some of these data will not be perceived as errors for the software operation. A transient error in a logic circuit might not be captured in a memory circuit because it could be masked by one of the following three phenomena [132], [154]:

(i) *logical masking* [154]-[155] occurs when a particle strikes a portion of the combinational logic that can not affect the output due to a subsequent gate whose result is completely determined by its other input values. For example, if the strike happens on an input to a NAND (NOR) gate [as illustrated in Fig. 40(a)], but one of the other inputs is in the controlling state [e.g., 0(1) for a NAND (NOR) gate], the strike will be completely masked and the output will be unchanged (i.e., the particle strike will not cause a soft error).

(ii) *temporal masking* (or latching-window masking) occurs when the pulse resulting from a particle strike reaches a latch, but not at the clock transition where the latch captures its input value [154]. This is

explained in Fig. 40(b): when the transient propagates towards a sequential element [a latch in Fig. 40(b)], the disturbance on node DIN may be outside the latching window [156]. Hence, the error will not be latched, and there will be no soft error.

(iii) *electrical masking* occurs for transients with bandwidths higher than the cutoff frequency of the CMOS circuit. These transients will be then attenuated [157]. The pulse amplitude may reduce, the rise and fall times increase, and, eventually, the pulse may disappear [as shown in Fig. 40(c)]. On the other hand, since most logic gates are nonlinear circuits with substantial voltage gain, low-frequency pulses with sufficient initial amplitude will be amplified [132].

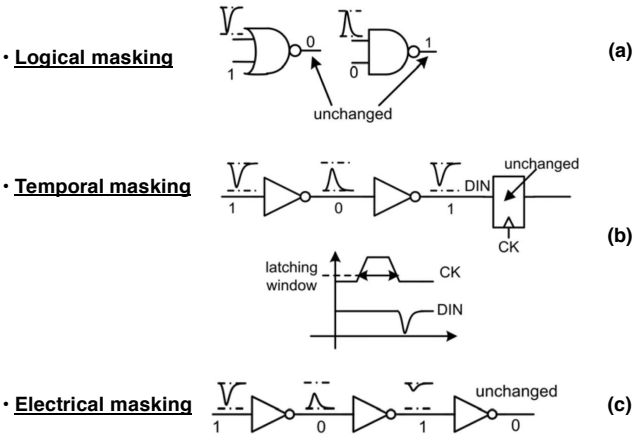

Fig. 40. Illustration of the masking phenomena in combinational logic. Adapted after Karnik *et al*. [132]. © 2004 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

Due to these masking effects the soft error rate in combinational logic was found to be significantly lower than expected [132], [154], [156]. Additional to these masking mechanisms, two key-factors impact the soft error rate in combinational logic: the clock frequency and the SET pulse width [141]. With increasing clock frequency there are more latching clock edges to capture a pulse and then the error rate increases. The pulse width is a key parameter which determines both the distance the SET will travel through the combinational chain and the probability that the SET be latched in a memory element as wrong data [142]. The wider the SET pulse width, the greater probability it has of arriving on the latching edge of the clock. If the transient becomes longer than the time period of the clock, then every induced transient will be latched [147]. The SET pulse width and amplitude depend on both process and circuit parameters (substrate and/or epitaxial layer doping, circuit capacitance, etc.) [148].

C. SER scaling trends in combinational logic

DSETs mechanisms, their production and propagation, as well as their effects on logic circuits have been extensively addressed in previous experimental and modeling works [141]-[174]. Some of these works highlighted that DSETs have always been occurring in combinational logic, but their impact was minor in old technologies (due to the three masking effects discussed above). Then combinational logic was in the past much less susceptible to soft errors than memory elements [154]. Nevertheless, as CMOS technology scales down, soft errors in digital circuits become a great concern, as it was shown in a recent work [154], where it was predicted that by 2011 the soft error rate in combinational logic will be comparable to that of unprotected memory elements. Several reasons explain this trend:

(i) The technology scaling allows more transients having sufficient pulse width and amplitude to be captured. Compared to older technology nodes, the advanced deep sub-micron technologies are capable of capturing a substantial fraction of SETs due to their higher operating frequencies. For combinational logic the SER is linearly dependent on frequency for transients shorter than the clock periods [147].

(ii) When the circuit speed increases, the ability of transients to propagate through the circuit increases [15].

(iii) With decreasing feature sizes the charge representing a logic “high” state decreases, resulting in an increased number of SETs [149].

Finally, the recent examination of the digital SET pulse width and cross-section as a function of technology node indicates that the pulse width strongly depends on the nominal operating voltage; the

pulse width could potentially increase with decreasing the feature size due to the concomitant decrease in the operation voltage [148]. This increase of the pulse width will further increase the soft error rate in future scaled digital circuits. For advanced technologies, the errors due to DSETs are expected to dominate the overall error rate of the entire circuit [141]; the primary source of errors in these circuits would then move from the static logic cells to combinational logic cells.

IV. ILLUSTRATION AT CIRCUIT LEVEL AND PREDICTIONS WITH TECHNOLOGY SCALING FOR DIGITAL CIRCUITS

A. Simulation of DSET in inverter delay chains

The production and propagation of DSETs in scaled Silicon CMOS digital logic circuits has been recently studied by Dodd *et al*. using mixed-level simulations [15], [140]. The circuit used for this purpose is a delay chain containing ten inverters (Fig. 41) and the ion strikes the NMOS transistor of the first inverter. This transistor is modeled in the 3-D device domain, whereas all others devices are modeled at circuit level. The 10-inverter chain is followed by a broadening inverter and a set-reset latch. The later is used to latch the ion-strike induced voltage transient and the former is designed to increase transient widths (and to increase their probability to be captured by a latch) [140]. Both bulk and body-tied SOI CMOS technologies are considered in the simulation. For each technology, the ion has been considered to strike the most sensitive region: the drain for bulk technologies [165] and the middle of the gate in SOI technologies [140]. The simulated irradiation track was considered with a Gaussian shape with a characteristic radius of 0.1 μm and a Gaussian time dependence, centered on 200 fs and with a characteristic decay time of 100 fs; the ion LET was considered constant along the ion path. An example of the simulated output node voltages as a function of time is presented in Fig. 42 for bulk technology and for a LET = 7 MeV/(mg/cm^2). One can observe that the SET easily propagates without significant attenuation through the entire inverter chain and is captured as an SEU by the set–reset flip-flop. The critical LET required for unattenuated (or free) propagation is plotted in Fig. 43 for both bulk and SOI technologies as a function of the technology node. Fig. 43 shows that, as expected, the critical LET decreases with the transistor feature size for both SOI and bulk circuits. For 100 nm gate length the critical LET for bulk CMOS technology drops below the α particle maximum LET [2 MeV/(mg/cm^2)]. Finally, the SOI CMOS has a much better immunity to DSET than bulk counterparts, since higher LETs are needed in SOI to produce long transients that can propagate freely [140]. Simulations predict more than a three-generation improvement in critical LET in SOI compared to bulk Silicon circuits.

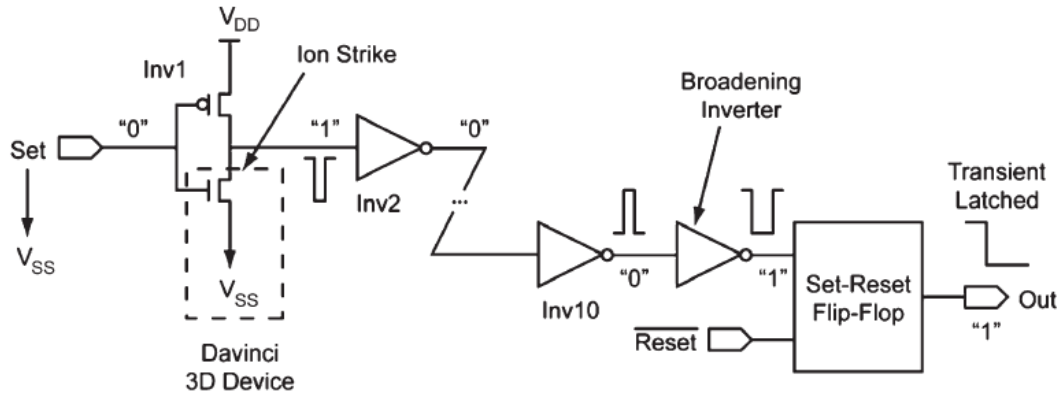

Fig. 41. Modeling technique for simulating a ten-inverter delay chain. The strikes to the n-channel transistor in the first inverter of the chain are modeled in the device domain (with Davinci tool) while the rest of the circuit is modeled within the circuit domain. After Dodd *et al*. [140]. © 2004 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

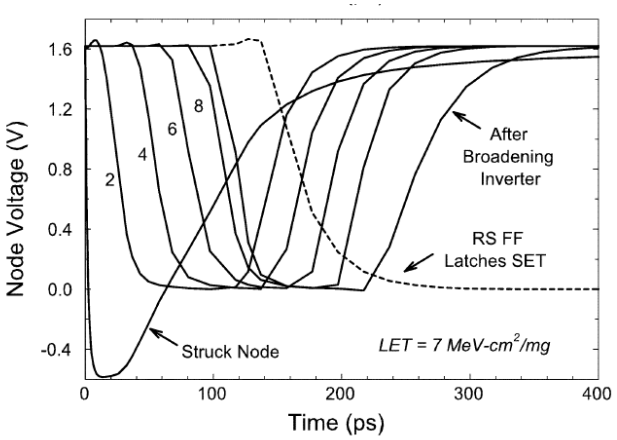

Fig. 42. Single-event transient propagation in 10-inverter delay chains at the 0.18 μm bulk CMOS technology node. After Dodd *et al*. [140]. © 2004 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

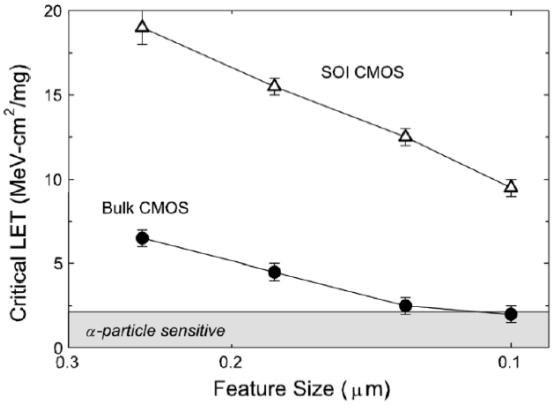

Fig. 43. Critical LET for unattenuated transient propagation as a function of scaling for bulk and SOI CMOS technologies. After Dodd *et al*. [140]. © 2004 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

Recently, the curve of the critical LET as a function of the feature size (Fig. 43) has been extended by Ferlet-Cavrois *et al*. in [174] until 70 nm gate length in partially-depleted SOI MOSFETs. In that work, circuit-level simulation of a 10 inverter chain has been performed (with Eldo) using measured transients as input stimulus. Although partially-depleted SOI MOSFETs exhibit low critical LET (similar to the curve concerning bulk Silicon devices in Fig. 43) due to the floating body, the results are consistent with simulations obtained by Dodd *et al*. in [140]. Ferlet-Cavrois *et al*. show that the critical LET continue to decrease with the technology scaling below 0.1 μm gate length.

B. Modeling the SER of flip-flop circuits

Modeling the SER of flip-flop circuits is more complex than that of SRAM cells because the critical charges for the flip-flop have to be weighed by different active areas at each sensitive node. SPICE simulations of flip-flop and SRAM performed for a 130-nm CMOS technology (supply voltage of 1.2 V) show that for most sensitive nodes, the critical charge for the flip-flop have the same order of magnitude as for the SRAM cell [153]. These results are resumed in Table I. Q_{crit} in flip-flop are in average slightly higher than in SRAM due to both the larger sizing of the transistors and higher inverter strengths (which differ from master to the slave) in the flip-flop design.

Table I. Critical charges in a 130nm CMOS flip-flop and regular SRAM cell. See Fig. 39 for the definition of the sensitive nodes. After Roche and Gasiot [153]. © 2005 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

	Sensitive node	Logic state	Q_{crit} (fC)
Flip-flop latch Master	MN	1	1.6
	M	0	2.8
	MN	0	3.3
	M	1	11.6
Flip-flop latch Slave	SN	1	2.4
	S	0	3.2
	SN	0	4.7
	S	1	15.6
SRAM		1	2.5

In order to compute logic SER of flip-flops in static mode two modeling methods have been used by Roche and Gasiot in [153]. In a first time, the entire flip-flop circuit was simulated in the 3-D device domain using commercial simulator [36]. Fig. 44 shows the simulated 3-D structure of the flip-flop circuit presented in [153] and generated using a 130-nm CMOS library composed of more than 500 000 finite elements meshed in 3-D. As already noted before in this short-course, this approach is the most accurate for the evaluation of soft error rates, but is very CPU time consuming.

A much faster solution is to use the empirical analytical model proposed by Hazucha and Svensson [135] (described in paragraph II). Since combinational and memory elements existing in modern processors are constructed from the same basic devices (NMOS and PMOS transistors), models developed for estimating the SER in memory elements can be used to assess soft errors in logic elements. Then the Hazucha and Svensson model has been used in [153] for evaluating the SER in flip-flop circuits. The results are presented in Fig. 45 and compared to experimental measurements (in arbitrary units) with alpha particles impacting the first-in first-out (FIFO) shift registers. Excellent agreement between the predictions derived from equation (26) and the experimental data is found. Results are also consistent with the critical charge presented in Table I; the higher the critical charge the lower the flip-flop SER.

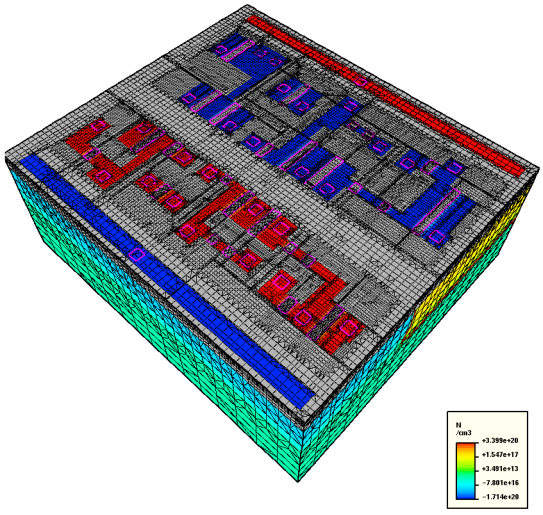

Fig. 44. Flip-flop modeled in one contiguous 3-D domain for SER studies. P and N diffusion areas respectively appear in blue and red. The N-well is depicted in yellow, the oxide trenches and gates in light grey. After Roche and Gasiot [153]. © 2005 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

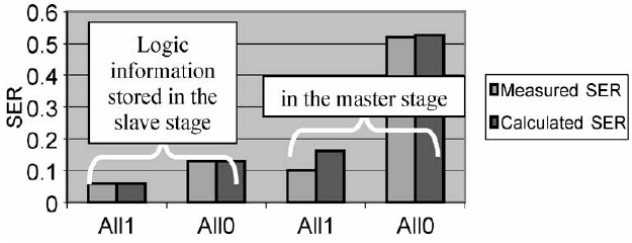

Fig. 45. Relative comparison of experimental measurements on a 130nm CMOS flip-flop and predictions with the Hazucha's empirical formula. After Roche and Gasiot [153]. © 2005 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

C. SER estimation in a logic chain

The impact of technology scaling on the soft error rates in CMOS memory, latches and combinational logic circuits was thoroughly examined by Shivakumar *et al.* in [154]. The SER is calculated using an end-to-end model, which captures the effects of two important masking phenomena: electrical masking and latching window masking. As noted previously, these phenomena are recognized as inhibiting soft errors in combinational logic and have to be taken into account in the SER evaluation. The SER is estimated using analytical models for each stage the pulse passes from its creation to the time it reaches the latch, as shown in Fig. 46. In the first stage the charge generated by the particle strike produces a current pulse, which is then converted into a voltage pulse after traveling through a gate in the logic chain. The electrical masking model simulates the degradation of the pulse as it travels through the gates of the logic circuit. A model for the latching window determines the probability that the pulse is successfully latched. Finally, the combinational logic SER was estimated using an extended version of the Hazucha and Svensson model.

The SER was calculated for SRAM cells, latches, and logic circuits for feature sizes from 600 nm to 50 nm. Figure 47 shows the critical charge for SRAM cells, latches, and logic circuits, as well as the charge collection efficiency (Q_S), as a function of the technology node. The critical charge of logic circuits decreases more rapidly with feature size than the Q_{crit} of memory elements. By the 130 nm node the critical charge of latches converges to about the same values as SRAMs (which is in agreement with the example given in Table I [153]). The steep reduction in Q_{crit} for logic circuits is primarily due to quadratic decrease in node capacitance with feature size. Since logic transistors are typically wider than

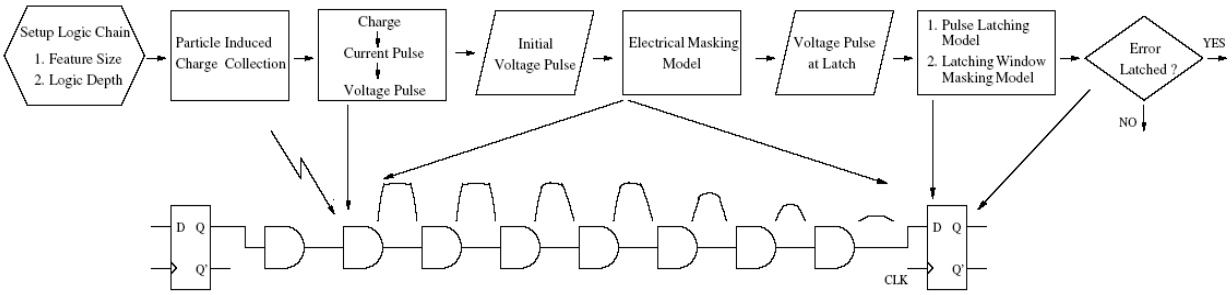

Fig. 46. Process for determining the soft error rate in a logic chain. After Shivakumar *et al*. [154]. © 2002 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

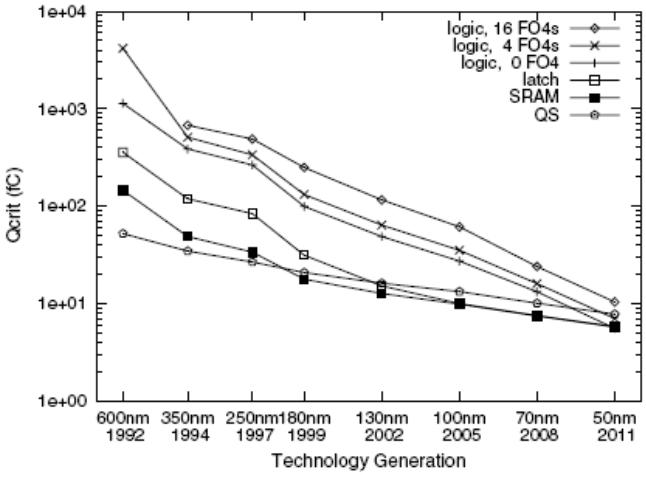

Fig. 47. Critical charge for SRAM/latch/logic as a function of the technology node. The labels "Logic" stand for static NAND gates with a fan-out of 4 and various pipeline depths. "Q_S" is a simulation parameter corresponding to the charge collection efficiency in the device. After Shivakumar *et al*. [154]. © 2002 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

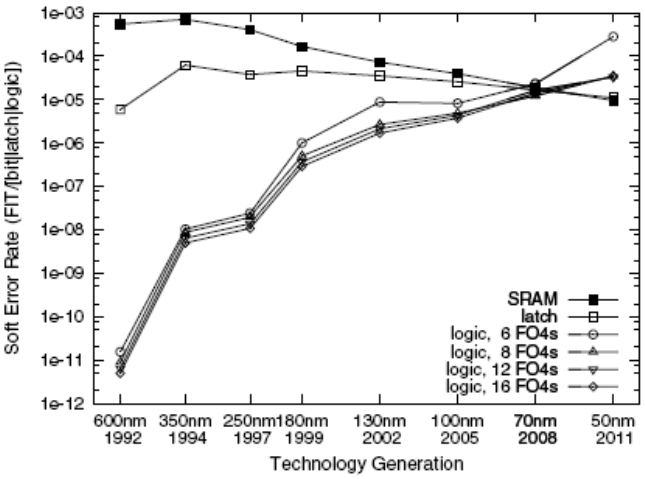

Fig. 48. SER as a function of the technology node for SRAM, latches and logic individual devices. After Shivakumar *et al*. [154]. © 2002 Institute of Electrical and Electronics Engineers Inc., reproduced with permission.

transistors used in memory circuits (where density is important), this effect is more pronounced in logic circuits [154].

The predicted SER for each class of circuits is plotted in Fig. 48. The SER of a single SRAM cell declines gradually with decreasing device size, while the SER of a latch stays relatively constant. The Q_{crit}/Q_S ratio for latches is larger than for SRAMs at large feature sizes, but Q_{crit} of latches decreases more rapidly than SRAMs with decreasing feature size. This explains the relatively small change in the SER for a single latch shown in Fig. 48. A continuous significant increase in SER (over five orders of magnitude from 600 nm to 50 nm technology nodes) is observed for a single logic chain. This is primary

due to the reduction in Q_{crit} of logic circuits with decreased feature size. Since the SER depends exponentially on the $-Q_{crit}/Q_S$ ratio [Eq. (26)], when this ratio is large, the factor $\exp(-Q_{crit}/Q_S)$ dominates the SER expression, but its influence decreases rapidly as the value of Q_{crit} approaches Q_S. Similar results are found in [175], where the considerably increase of the logic-SER with downscaling is also highlighted.

Finally, an interesting prediction of the work of Shivakumar *et al*. [154] is that the SER per chip of logic circuits will increase nine orders of magnitude from 1992 to 2011 and will be comparable to the SER per chip of unprotected memory elements (as shown in Fig. 48). In conclusion, computer system designers must absolutely address the risks of soft errors in ultra-scaled logic circuits predicted for the future technology nodes.

SUMMARY

The status of research in modeling and simulation of single-event effects (SEE) in digital devices and integrated circuits was reviewed in this short-course. We particularly emphasize on the current challenges concerning the physical modeling of ultra-scaled devices (in the deca-nanometer range) and new device architectures: Silicon-on-insulator, multiple-gate and Silicon nanowire MOSFETs. The growing interest in simulation relies on its numerous capabilities: insight into device behavior due to the possibility of "observing" physical quantities that can not be measured on real devices, predictive capability which may reduce radiation experiments, capability to perform "what if" studies, which are not feasible experimentally. With reducing the feature sizes and the emergence of new devices, such as multiple-gate or Silicon nanowire transistors, device integration becomes more and more difficult and manufacturing processes more and more complex and exponentially expensive. In this context, simulation offers then the unique opportunity to investigate, in advance of process integration, the radiation effects in these ultimate devices, study which can be difficult, very expensive and less rapid in experiment. Since computers are considerably cheaper resources, simulation is becoming an indispensable tool for the study of the device sensitivity to ionizing radiation.

In the past decade, substantial progress has been made in numerical methods and computer performances, which make possible to perform heavy 3-D simulations of SEE in relatively short time. With the reduction of devices feature size in the deca-nanometer range, current challenges concern the accuracy of the physical models used in simulation of SEE. Although advanced models taking into account non-stationary effects and quantum confinement are currently available, emerging quantum transport phenomena, predicted for gate lengths below 30 nm, still have to be considered. The impact of these phenomena (including ballistic and quasi-ballistic transport and quantum tunneling) on the sensitivity to single-event of digital devices and circuits is presently an open question which needs to be addressed in future simulation studies.

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